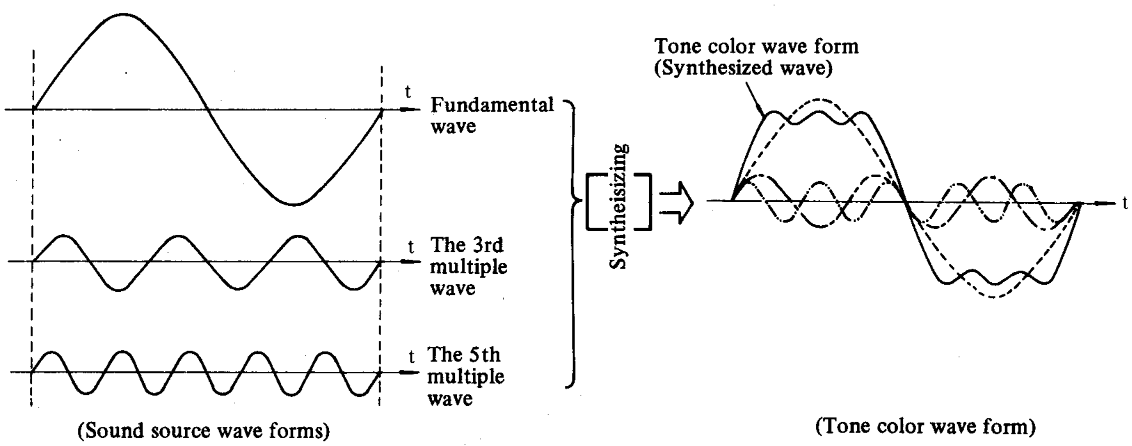
I. OUTLINE

1 ● OUTLINE OF CIRCUIT SYSTEM

Generally, the electronic organ produces various tones based on one kind of sound wave. There are two systems for producing these tones.

1. Synthesizing System (Sine Wave Synthesizing System)

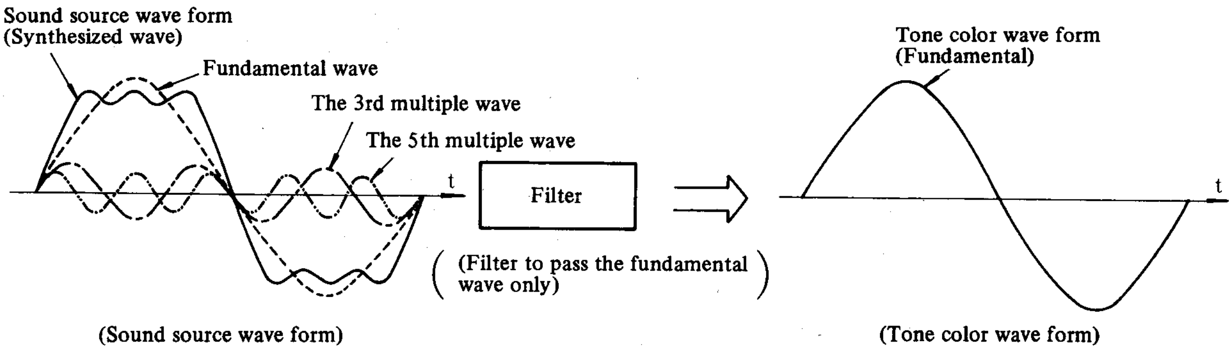
The synthesizing system is the standard way to produce tones by preparing numbers of pure sounds (sine wave) related to overtones and synthesizing them. But the circuits limit the number of tones with plenty of overtones (i.e. string-like sound) that can be produced, therefore the system is used for special Electone (Model F-1).



[Fig. 1]

2. Filter System

Tones with complicated overtones such as sawtooth waveshape are produced as sound source. They are filtered through filter circuit to create the tones with respective frequency characteristics. In this way a large number of tones could be produced uniformly.



[Fig. 2]

- These two systems have their own good features. However, some tones might be hard to produce through conventional system which has been creating all the tones with one kind of sound source. (Refer to Figure 3) Because the overtones contained in the sound signals are fixed and also the number of overtones is limited accordingly.

Sound source wave forms \ Tone color	Flute	Oboe	Clarinet	String	
Sine wave	◎	×	×	×	Synthesizing method
Saw tooth wave	○	◎	×	○	Filter method
Square wave	○	×	◎	×	
Asymmetrical rectangular wave	○	○	×	◎	

(Note) ◎ Easy to produce
○ Possible to produce
× Hard to produce

[Fig. 3] Sound source wave – Tone color relation

- Therefore, the PAS system Electone is designed and so constructed to produce many and rich tone colors by employing both of the tone creating methods (Synthesizing System and Filter System) according to each sound source waveshape. Naturally, several sound source waveshapes with their own peculiar overtones are generated and used according to tone color.
- Conventional electronic organs with oscillators as the sound source would require a complicated circuit if they were to have two differing methods to produce these tones, due to the method of creating the sound waves as well as to the key switches. With the PAS System organ, however, it is possible to process the two systems digitally.

By pressing down the single contact key switches a number of pure sounds (sine waves) related to overtones can be created at the same time. By synthesizing these sounds as desired a flute family tones can be produced, and at the same time a multiple number of sound source waves (sawtooth waves, square waves, and asymmetrical rectangular waves), each with their peculiar overtones, can be created, corresponding to the tone such as in the filter system.

Moreover, when VCF (Voltage Controlled Filter) is used for filter circuit, better natural sound can be created through the time shifting of harmonic spectrum.

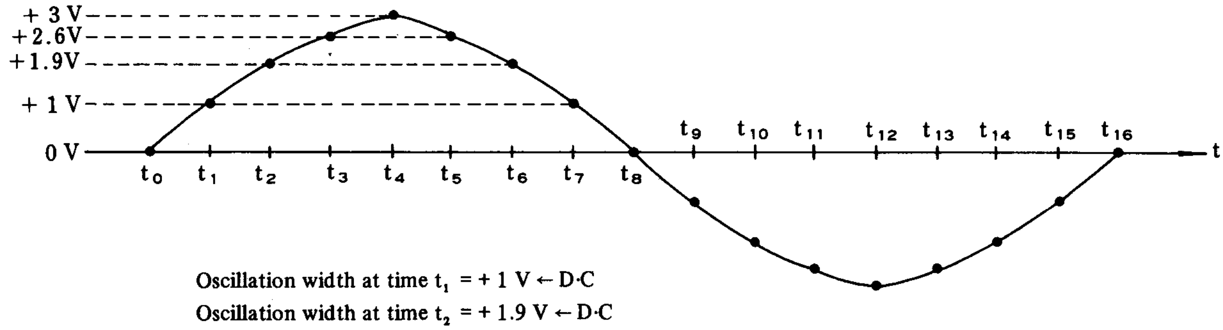
The following is an explanation of the principles of the sound source wave generation in the digital Electone, as well as an outline of the functions of the circuit.

2 ● PRINCIPLES OF GENERATION OF SOUND SOURCE SIGNAL (WAVE FORMS)

The sound source signal generation method of the digital system Electone differs completely from the conventional method where an oscillator is used as the sound source. For example, when looking at a certain sine wave, there will be a moment when the oscillation width can be read as a direct current value. As this direct current successively changes, a single sine wave is formed.

Example 1

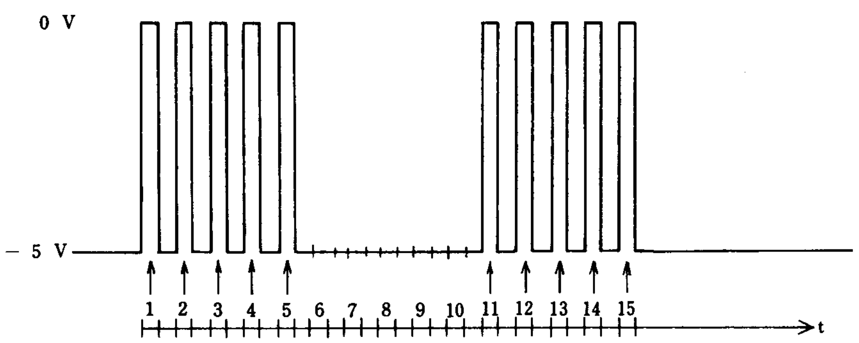
In the case sine wave with maximum 6V of amplitude is divided on time axis:



[Fig. 4]

Therefore, here a fine division has been prepared in advance between the two voltages as the momentary oscillation width voltage for the sound source wave pattern. To obtain the desired wave pattern from this divided voltage, read every 12μS in the order the sampled voltage. The oscillation width will gradually change, and as a result a single wave pattern will form.

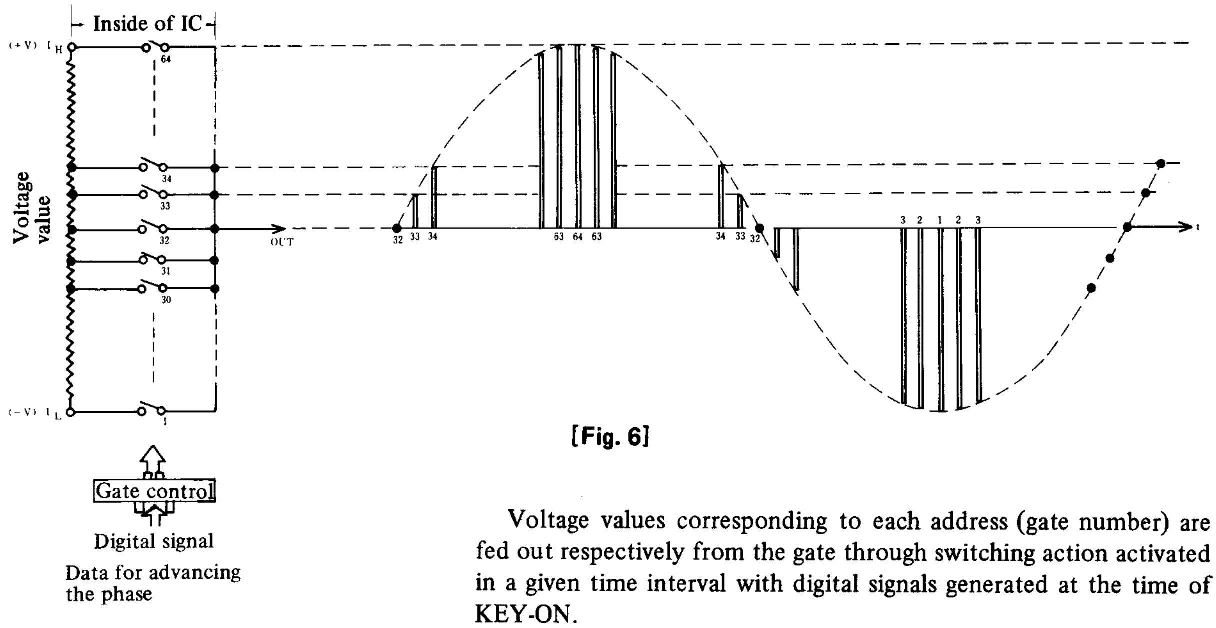
[Example 2] Wave form of rectangular wave with maximum oscillation width 5V.



[Fig. 5]

On PAS system Electone, as shown in the figure (Example 3), the voltage applied to the terminals I_H and I_L is finely divided so that the wave patterns will be of the respective sampling oscillation width value at the time of time sharing. Each sampling point, thus, can be obtained as desired through a switching action with digital data (frequency data) of 1μS width pulses generated each 12μS periodically.

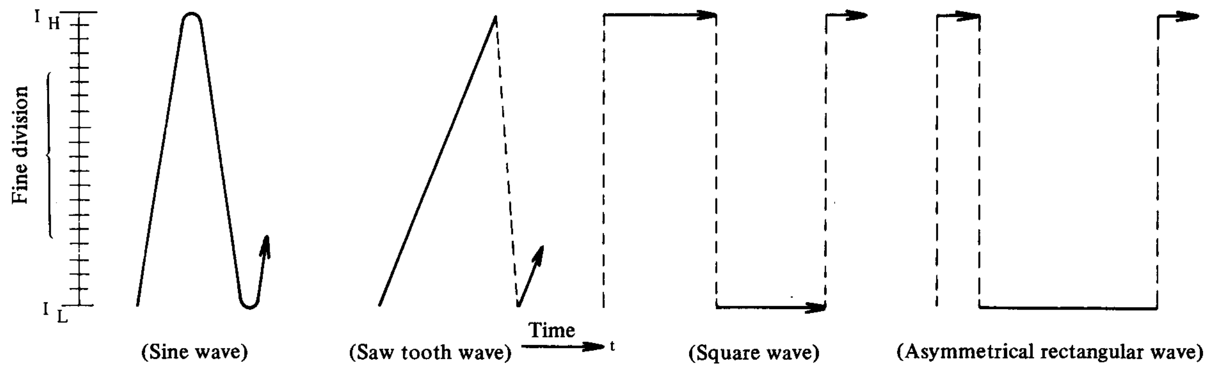
[Example 3] Principle of sine wave generation on PAS System Electone.



[Fig. 6]

Voltage values corresponding to each address (gate number) are fed out respectively from the gate through switching action activated in a given time interval with digital signals generated at the time of KEY-ON.

Of course, the procedures for reading will differ according to the wave pattern.

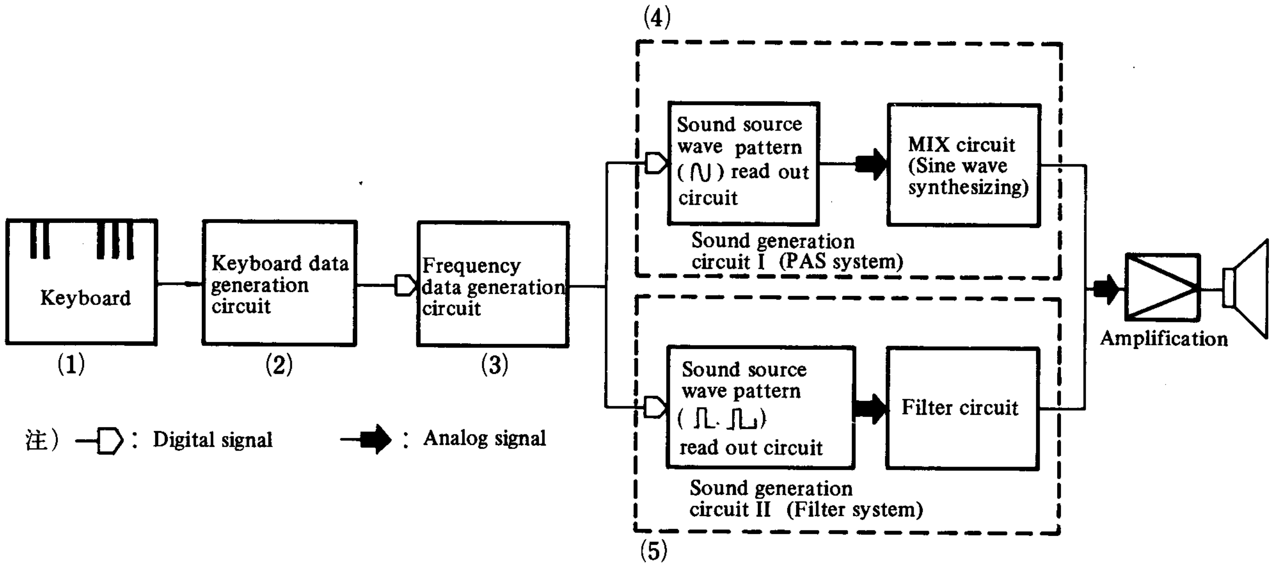


[Fig. 7] The procedures for reading of sampling voltage

This sampling voltage is read every 12μS. The digital signal is produced as frequency data matching the key pressed.

3 ● OUTLINE OF THE CIRCUIT FUNCTION

An outline of the circuit construction of PAS System Electone is as shown in Fig. 8.



[Fig. 8] Outline of circuit construction of PAS System Electone.

• OUTLINE OF MOVEMENTS

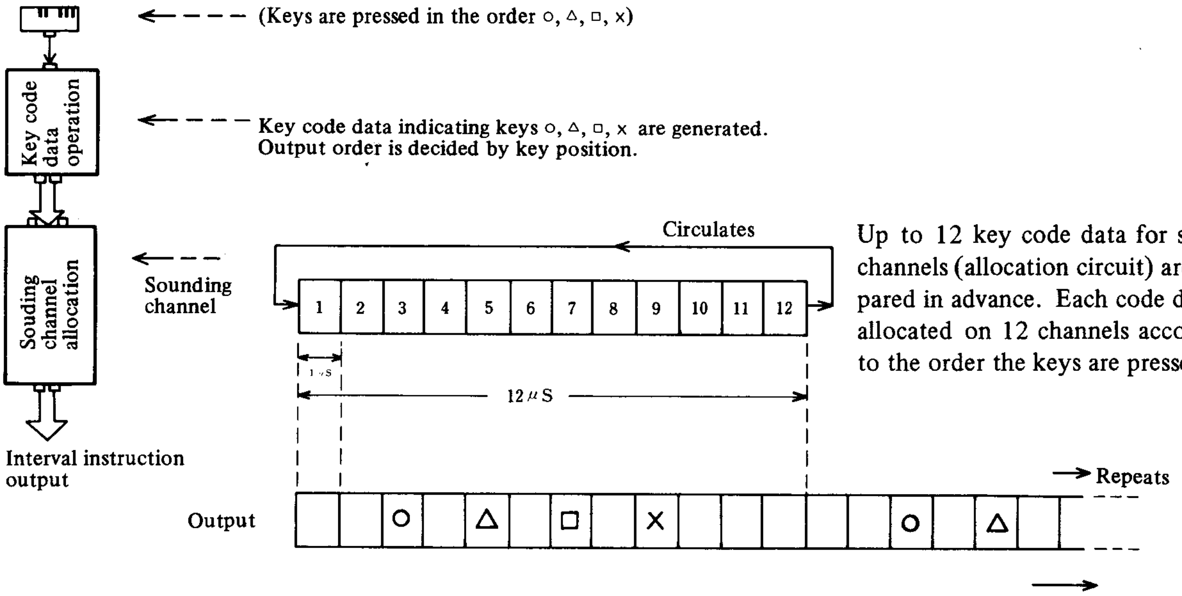
1. Keyboard

The keyboard uses only single contact switches.

2. Keyboard Data Generation Circuit

This circuit is functionally divided into two parts: One part for preparing the key code data indicating the key pressed and the other part for preparing the phonetic control data to process the key data.

First, when the key is pressed (the key switch will be in contact) the pressed key will be detected and the key code data indicating that key will be generated in order through time sharing. Moreover, a maximum of up to 12 key code data will be allocated on 12 channels, according to the order the keys are pressed, prepared in advance as the key code data (instructing the frequency of the sound source). The key code data allocated on this phonetic channel is output on the following frequency detection circuit as interval instructions to create the sound frequency corresponding to the key indicated by the data.



[Fig. 9]

Up to 12 key code data for sound channels (allocation circuit) are prepared in advance. Each code data is allocated on 12 channels according to the order the keys are pressed.

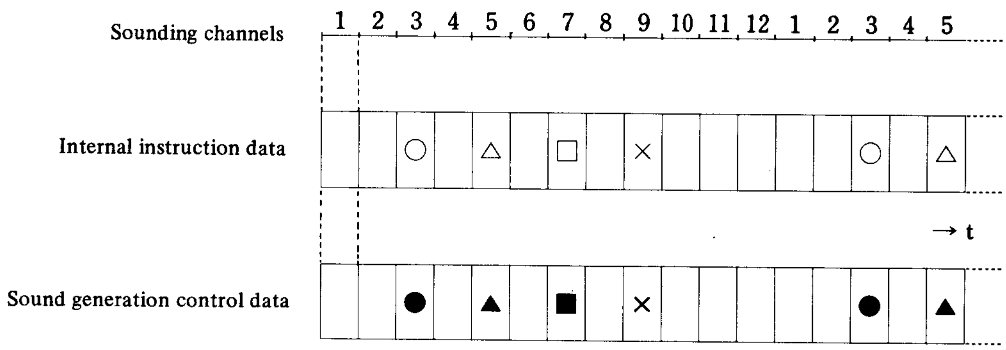
Time is divided into 12 channels by each 1μ second and the channels are processed through time sharing.

Therefore, key code data allocated to each sounding channel are repeatedly output by every 12μ seconds. The code data are added to Frequency Data Generation Circuit to determine the frequency.

Also, and at the same time, sound control data are produced synchronously to the phonetic instruction data of each sound generating channel.

According to this data, the key sound allocated to each channel will be controlled. (with this, a maximum of 12 sounds can be produced at the same time.) **(12-sound Time Sharing)**

Keyboard data generation circuit output



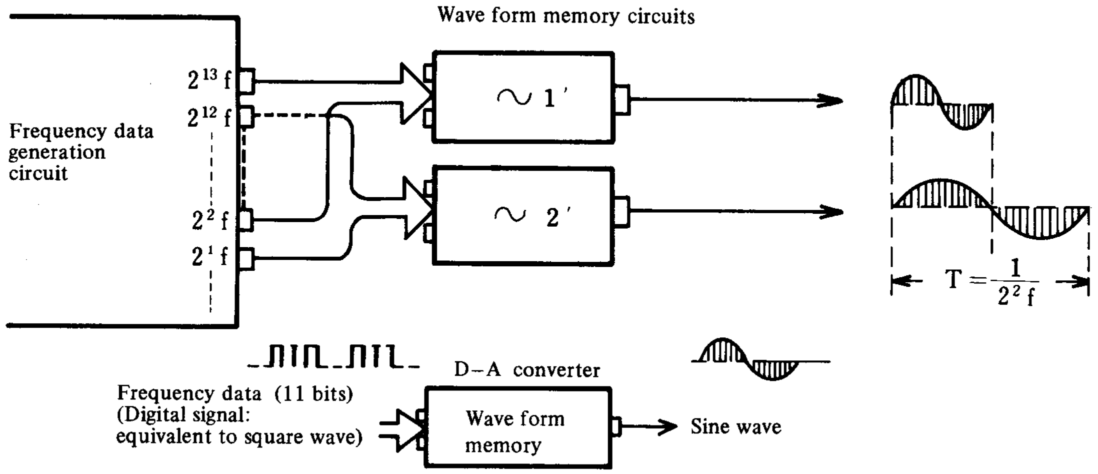
[Fig. 10]

3. Frequency Data Generation Circuit

This circuit receives the interval instruction data and produces a number of frequencies at the same time, related to the interval frequency of the key indicated by the data as well as the overtones. The frequencies produced here are ¼f, ½f, 2^0f, 2^1f, 2^2f . . . . . 2^{13}f, or 16 bits for the basic frequency. By reading out the interval wave pattern for 11 bits and adding this to the circuit, the interval wave pattern can be read. This frequency is all shown digitally. (However, to the eye it appears to be a square wave) **(12-sound time sharing)**

4. Tone Generation Circuit (PAS System)

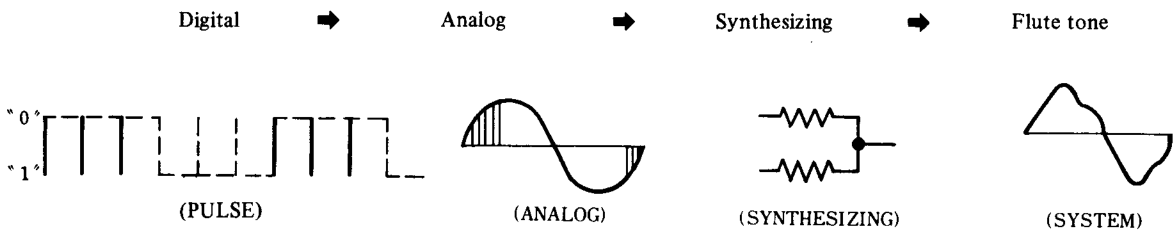
This circuit serves the function of producing a flute sound source by creating a number of sine waves related to overtones and mixing them in at the proper time. First, a sound source wave form memory circuit is prepared in advance according to the number of couplers. Then by connecting them as shown below for 11 bits of frequency data, the sine waves of the frequency related to the overtone will be created in the same number as the wave form memory circuit.



[Fig. 11]

In this way, in order to make the sine wave which has been originated into a flute sound, levelling adjustment as well as synthesizing is carried out in the MIX circuit. **(12-sound time sharing)**

Thus the frequency corresponding to the key pressed is produced digitally (pulse). By converting this to analog voltage, a sine wave can be originated. The method where the tone is produced through synthesizing is referred to as the PULSE ANALOG SYNTHESIZING SYSTEM (abbreviated as System.)



[Fig. 12]

5. Sound Source Generation Circuit (Filter System)

This circuit functions to produce tones from three kinds of interval wave patterns (sawtooth waves, square waves, and asymmetrical rectangular waves), with each containing its own unique overtone composition and adding them to the filter circuit.

Here the original note receives the frequency data of 10 bits from the frequency data generation circuit mentioned in (3) above, to create the sound source wave form.

Moreover, this filter system is classified according to whether the frequency characteristics of the tone circuit forms a fixed filter (Formant system), or whether a voltage control filter (VCF) is used to permit the frequency characteristics to be altered by voltage.

6. Amplifying Circuit

This circuit mixes the sound produced simultaneously in the sound source generation circuit I and II, amplifies it and sends it to the speaker. Circuits come after this circuit is designed to have the same construction as conventional Electone.

(Reference)
Tone colors are named on PAS System Electone as follows:

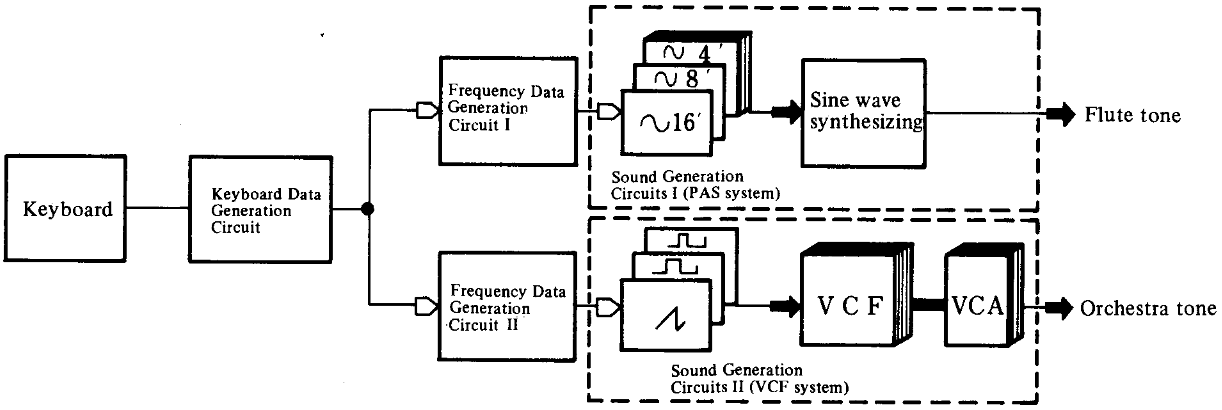
- "Orchestra Tone" towards the tone colors produced through VCF (Voltage Controlled Filter)
- "Complex Tone" towards the tone colors produced through filters (FORMANT)
- "Flute Tone" towards the tone colors produced by synthesizing sine waves.

4 ● CLASSIFICATIONS OF PAS SYSTEM ELECTONE

All Electones using the digital system have two differing note production circuits to create the respective sounds within the same musical instrument.

1. PAS–VCF Type

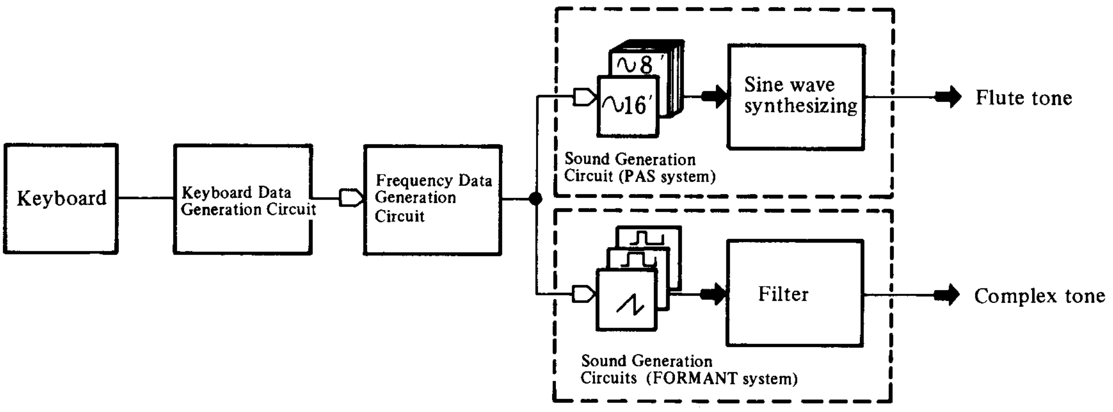
The type constructed to produce both a flute tone under the PAS system and the orchestra tone under the VCF system is referred to as the PAS–VCF Electone.



[Fig. 13] Outline of PAS–VCF

2. PAS–FORMANT Type

An Electone which produces the flute tone through the PAS system but other tones through the Formant system is referred to as the PAS–FORMANT type Electone.



[Fig. 14] Outline of PAS–FORMANT

PAS System Electone organ is the general name for these two systems.

II. CIRCUIT MOVEMENT

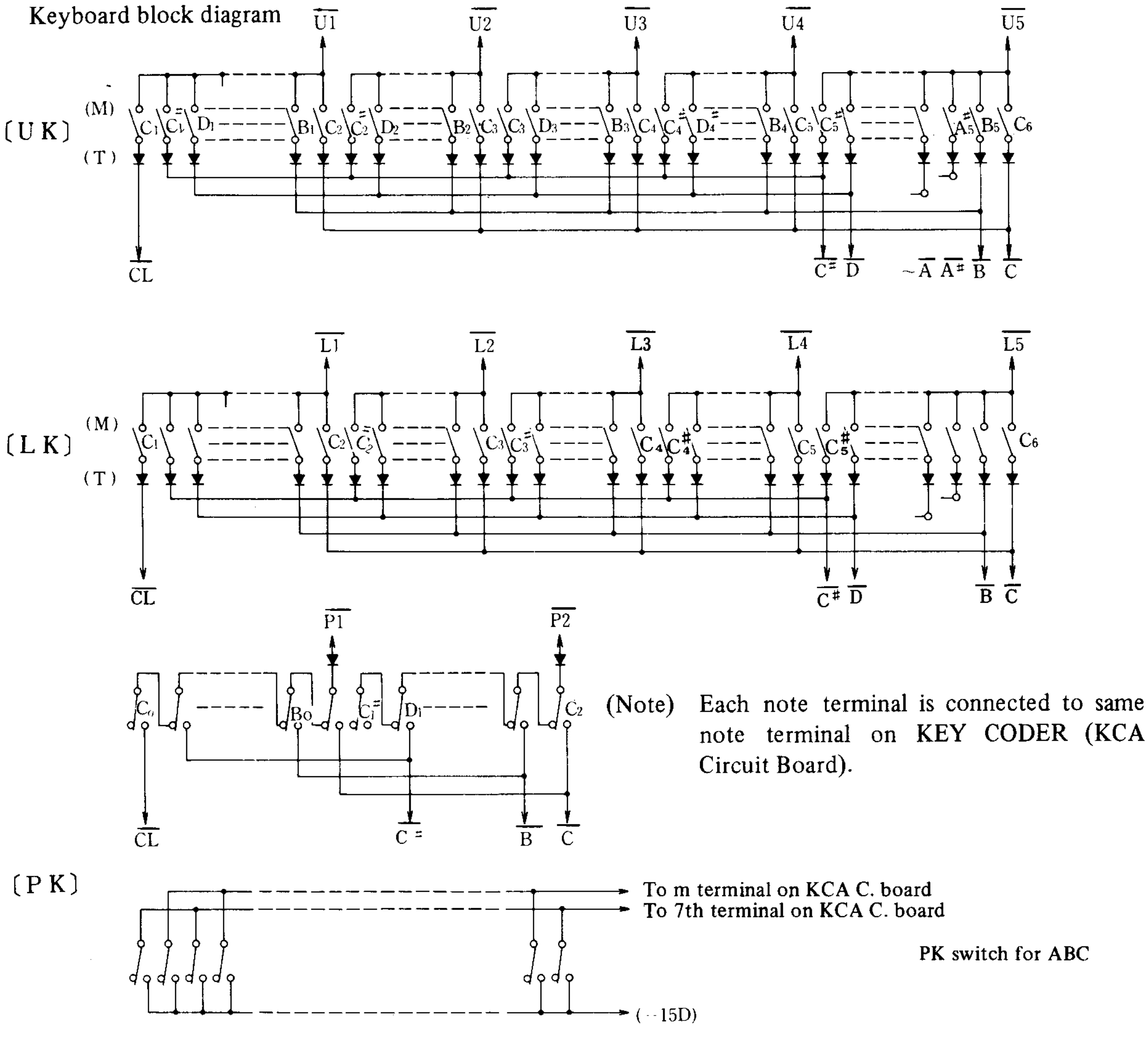
1 ● KEYBOARD

- The keyboard of the Electone using the digital techniques informs the position (kind of sound) of the key pressed to the KEY CODER. Thus, as this keyboard only has an ON/OFF function all the key switches are of the single contact type.

- This keyboard, as can be seen in (Fig. 15), is divided into blocks for each octave ($C^{\#} \sim C$) designated as UK, LK and PK. The key switch for each block is divided by notes and through a combination of these two groups, i.e. 'blocks' and 'notes', the individual key switches are identified.

- That is, the fixed contact points (M) of each key switch are divided into blocks by octave, while the variable contact points (T) are divided by notes. Similar notes have a common wiring and are connected to the terminals for each block (U1 ~ U5, L1 ~ L5, P1, P2) as well as to the terminals for the notes (C ~ CL) of the key coder prepared for each. With the combination of the block terminals and the note terminals through the contact of the key switches the key coder is informed of the position of the key which has been pressed.

Keyboard block diagram

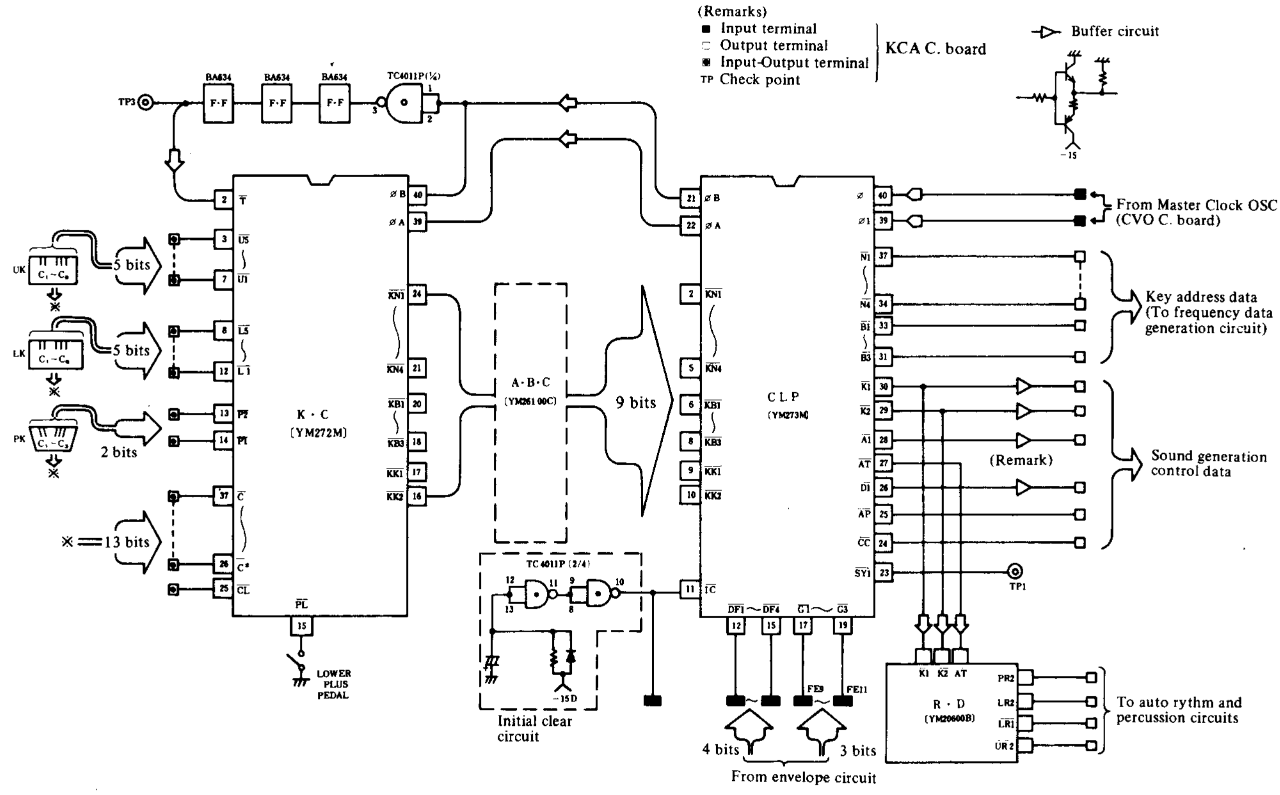


(Note) Each note terminal is connected to same note terminal on KEY CODER (KCA Circuit Board).

[Fig. 15] Keyboard Block Diagram

2 ● KEYBOARD DATA GENERATION CIRCUIT

The keyboard data, necessary for producing the sound corresponding to the key, is produced digitally in this circuit.



[Fig. 16] Basic block diagram of the keyboard data generation circuit on PAS—VCF

- The construction of the circuit is as shown in Fig. 16.
  - ○ Key Coder (K · C)
    To identify the keyboard switch which has been pressed from among the numerous switches, the Key Coder produces code data (key code data) the same number of times as the keyboard switches are pressed.
  - ○ Channel Processor (CLP)
    A maximum of 12 sounds can be received in the order the key code data is produced by the Key Coder and the key code instruction data received, as well as the sound envelope instruction data, among others, are prepared.

  Two intelligent ICs are used.

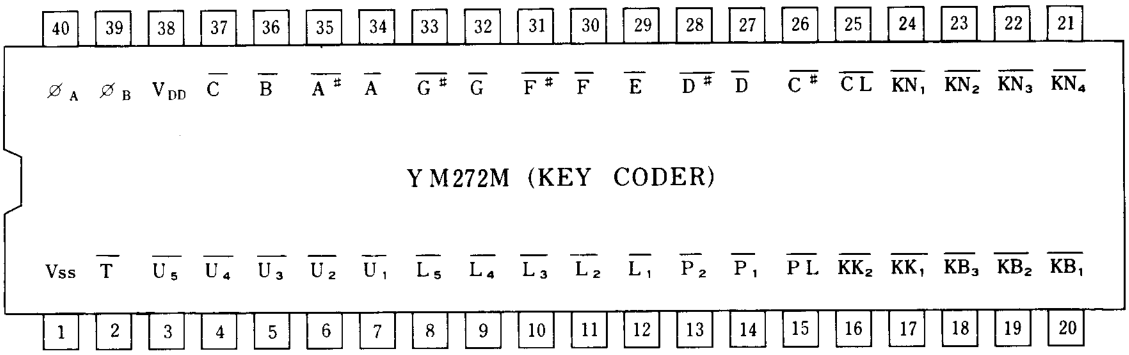
Moreover, the output data from the KC is input into the A·B·C circuit and then output to the CLP. When the A·B·C function is OFF, the data enters as is into the CLP. (Refer to A·B·C function for details)

2 — 1 ● KEY CODER (K · C)

1. Key Coder Points

1. Codes only the data indicating the keyboard switch which has been pressed.
2. The output is carried out progressively, in order of priority, according to a time sharing process.

2. Explanation of the YM272M (K · C) terminals



Terminal No.	Code	Designation	Significance	Terminal No.	Code	Designation	Significance
1	Vss	———	Power source (0V)	40	$\varnothing_A$	Master clock pulse (ϕA is opposite phase from ϕB)	IC movement clock (Defines IC operation and pulse width of Output Data, f ≒ 37 kHz
2	$\overline{T}$	TIMING CLOCK	f = $\phi B \times 1/8$ ≒ 4.6 kHz Data coding timing clock	39	$\varnothing_B$		
3	$\overline{U_5}$	UPPER 5	Keyboard block wiring UK Octave 5	38	V_{DD}	———	Power source (−15V)
4	$\overline{U_4}$	〃 4	〃 Octave 4	37	$\overline{C}$	———	Keyboard sound wiring
5	$\overline{U_3}$	〃 3	〃 Octave 3	36	$\overline{B}$	———	〃
6	$\overline{U_2}$	〃 2	〃 Octave 2	35	$\overline{A^\#}$	———	〃
7	$\overline{U_1}$	〃 1	〃 Octave 1	34	$\overline{A}$	———	〃
8	$\overline{L_5}$	LOWER 5	〃 LK Octave 5	33	$\overline{G^\#}$	———	〃
9	$\overline{L_4}$	〃 4	〃 Octave 4	32	$\overline{G}$	———	〃
10	$\overline{L_3}$	〃 3	〃 Octave 3	31	$\overline{F^\#}$	———	〃
11	$\overline{L_2}$	〃 2	Octave 2 of LK	30	$\overline{F}$	———	〃
12	$\overline{L_1}$	〃 1	Octave 1 of LK	29	$\overline{E}$	———	〃
13	$\overline{P_2}$	LOWER 2	Octave 2 of PK	28	$\overline{D^\#}$	———	〃
14	$\overline{P_1}$	〃 1	Octave 1 of PK	27	$\overline{D}$	———	〃
15	$\overline{PL}$	PEDAL to LOWER	Pedal sound with LK	26	$\overline{C^\#}$	———	〃
16	$\overline{KK_2}$	KEYCODER KEYBOARD·DATA2	KC key code data (2 bits)	25	$\overline{CL}$	———	〃
17	$\overline{KK_1}$	〃 1		24	$\overline{KN_1}$	KEYCODER NOTE·DATA1	Note data output (4 bits)
18	$\overline{KB_3}$	KEYCODER BLOCK·DATA3	KC block data (3 bits)	23	$\overline{KN_2}$	– do. – 2	
19	$\overline{KB_2}$	〃 2		22	$\overline{KN_3}$	– do. – 3	
20	$\overline{KB_1}$	〃 1		21	$\overline{KN_4}$	– do. – 4	

[Fig. 17]

3. Functions of the Key Coder

Each block terminal ($\overline{U_1} \sim \overline{U_5}, \overline{L_1} \sim \overline{L_5}, \overline{P_1}, \overline{P_2}$) of the Key Coder as well as each note terminal ($\overline{C} \sim \overline{CL}$) is connected respectively to one of the variable contact points ($\overline{T}$) and the fixed contact points (M) of the key switches. Therefore, when the key is pressed the block terminal and the note terminal corresponding to the key pressed will be in contact.

- Functions of the Key Coder

  The Key Coder detects which keyboard, UK, LK or PK, as well as the position (interval) of the key in contact with the block terminal and the note terminals. The key code data indicating the keys which have been detected are successively output through time sharing.

4. Key Code Data (Key Switch Identification Data)

The key code data which originates by pressing this key is made up of:

- Keyboard Code Data (which indicates the keyboard, i.e. UK, LK, or PK to which the key belongs)
- Octave Code Data (which indicates the octave of the keyboard to which the key belongs)
- Note Code Data (which indicates the note of the key)

As shown in (Fig. 18) there are 2 bits ($\overline{K_1}, \overline{K_2}$) for the keyboard data, 3 bits ($\overline{B_1} \sim \overline{B_3}$) for the octave data, and 4 bits ($\overline{N_1} \sim \overline{N_4}$) for the note data. When combined they make up 9 bits ($\overline{K_1} \sim \overline{N_4}$). This key data indicates which keyboard and the position of the key. That is, through a binary combination of "0" and "1" an identification of the key switch can be made.

○ Keyboard Code Data

Output terminal \ Keyboard	UK	LK	PK
$\overline{K_1}$	0	1	0
$\overline{K_2}$	1	0	0

(Note)

○ Octave Code Data

Output terminal \ Octave	OCT0 ($C_0 \sim C_1$)	OCT1 ($C_1^\# \sim C_2$)	OCT2 ($C_2^\# \sim C_3$)	OCT3 ($C_3^\# \sim C_4$)	OCT4 ($C_4^\# \sim C_5$)	OCT5 ($C_5^\# \sim C_6$)
$\overline{B_1}$	1	0	1	0	1	0
$\overline{B_2}$	1	1	0	0	1	1
$\overline{B_3}$	1	1	1	1	0	0

○ Note Code Data

Output terminal \ Note	C#	D	D#	E	F	F#	G	G#	A	A#	B	C (CL)
$\overline{N_1}$	1	0	1	1	0	1	1	0	1	1	0	1
$\overline{N_2}$	1	1	0	1	1	0	1	1	0	1	1	0
$\overline{N_3}$	1	1	1	0	0	0	1	1	1	0	0	0
$\overline{N_4}$	1	1	1	1	1	1	0	0	0	0	0	0

(Example 1) When UKA$_3$ key is pressed

When UK A$_3$ key is pressed

	Output terminal	Code	Wave form
Keyboard data	$\overline{K_1}$	0	⎍
	$\overline{K_2}$	1	—
Octave data	$\overline{B_1}$	0	⎍
	$\overline{B_2}$	0	⎍
	$\overline{B_3}$	1	—
Note data	$\overline{N_1}$	1	—
	$\overline{N_2}$	0	⎍
	$\overline{N_3}$	1	—
	$\overline{N_4}$	0	⎍

(Example 2) When LKA$_3$ key is pressed

When LK A$_3$ key is pressed

	Output terminal	Code	Wave form
Keyboard data	$\overline{K_1}$	1	—
	$\overline{K_2}$	0	⎍
Octave data	$\overline{B_1}$	0	⎍
	$\overline{B_2}$	0	⎍
	$\overline{B_3}$	1	—
Note data	$\overline{N_1}$	1	—
	$\overline{N_2}$	0	⎍
	$\overline{N_3}$	1	—
	$\overline{N_4}$	0	⎍

(Example 3) When UKC$_5$ key is pressed

When UKC$_5$ key is pressed

	Output terminal	Code	Wave form
Keyboard data	$\overline{K_1}$	0	⎍
	$\overline{K_2}$	1	—
Octave data	$\overline{B_1}$	1	—
	$\overline{B_2}$	1	—
	$\overline{B_3}$	0	⎍
Note data	$\overline{N_1}$	1	—
	$\overline{N_2}$	0	⎍
	$\overline{N_3}$	0	⎍
	$\overline{N_4}$	0	⎍

[Fig. 18] Code data

5. Principles of Movement (Refer to output timing chart)

The coding is carried out through four timed stages, according to Clock ϕ_B (≒ 27μS) and Clock $\overline{T}$ (≒ 215μS).
The timing indicates the coding action within the IC.
When the key is pressed Clock $\overline{T}$ will synchronize with ϕ_B when $\overline{T}$ starts to rise.
Stage (0) is the preparatory time.

Stage (1) is when all the note terminals have become −15V, the octave terminals and the note terminals belonging to the keys pressed are in contact, the OCT terminal is pulled to −15V, and the OCT memorized.

With stage (2) ' 0" voltage is added to the note terminals from the OCT terminal which has been noted, and the note memorized.

With stage (3) the memorized data are codified as data and output as $\overline{KK1}$, $\overline{KK2}$, $\overline{KB1}$ ~ $\overline{KB3}$, $\overline{KN1}$ ~ $\overline{KN4}$.

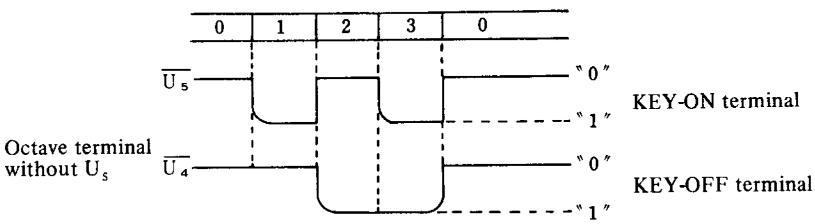
Once the key data has been output, the timing again returns to (0) and the procedures will be repeated as long as the key is being pressed. At this time, the coding action will again start when the Clock $\overline{T}$ pulse rises.

- Moreover. when more than two keys of the same keyboard and within the same octave are pressed there will be successive outputs in accordance with the order of priority in reading. (Repeat of timing (3)).
  And when all the data of the pressed keys have been output the timing will return to (0).
- Also when keys for more than two sounds of differing octaves are being pressed one sound data will be output according to the order of priority in reading, and then, after an interval (27μS), the next keyboard sound will be output.

*** Order of priority in reading**

①	②
U_5	C
U_4	B
U_3	A #
U_2	A
U_1	G #
L_5	G
L_4	F #
L_3	F
L_2	E
L_1	D #
↓ P_2	D
P_1	↓ C #

(Reference)
Voltage wave form on octave terminal when a key within U_5 is depressed.



[Fig. 19]

(Remarks) The coding action will stop when the key is released, but this output data will be memorized in the next CLP circuit.
To inform that the key has been released the following SL coding data will be sent for only one time (27μS) $\overline{T}$ x 8 after the key has been released.

- SL coding data

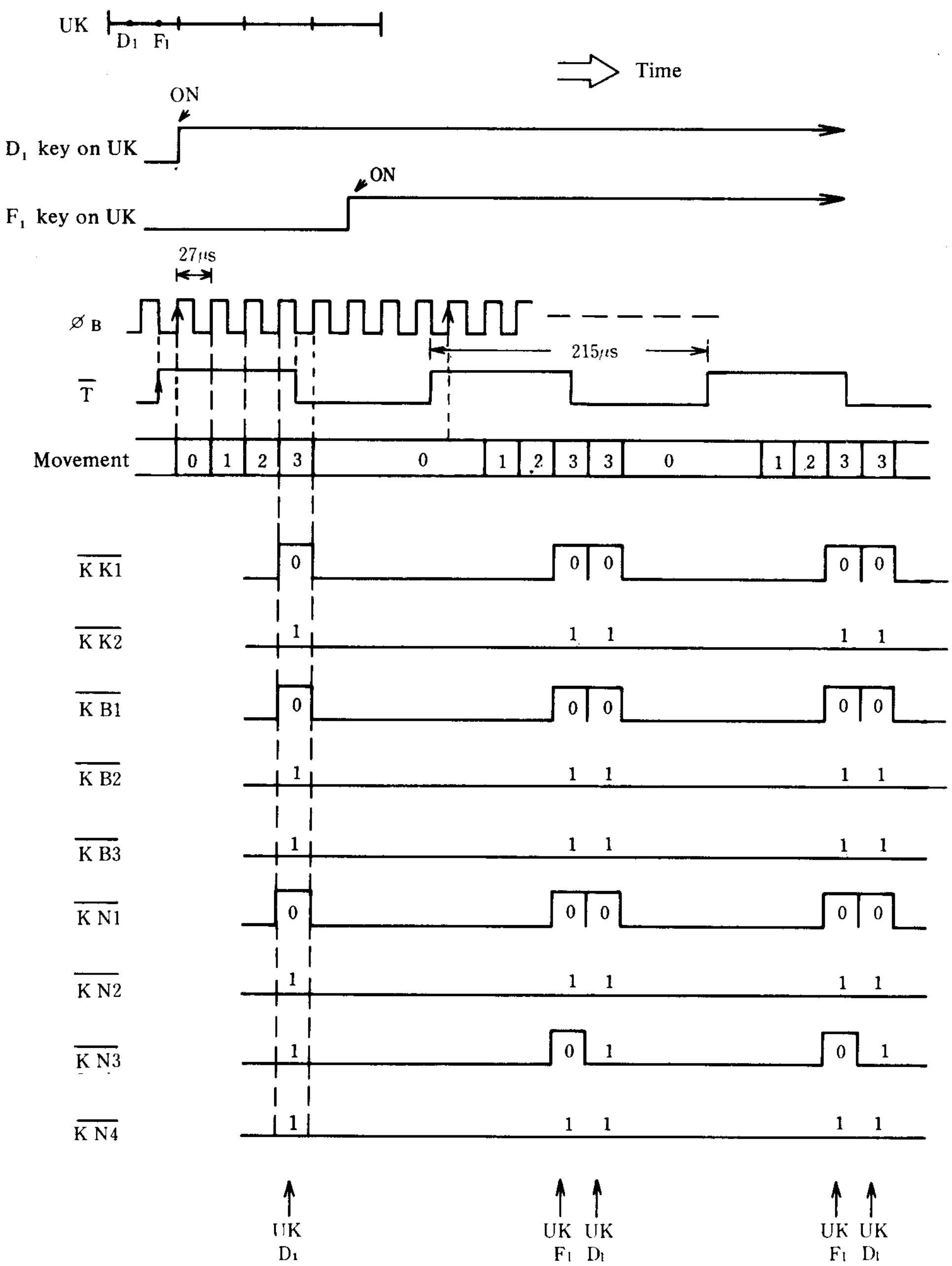
[Fig. 20]

	$\overline{K_1}$	$\overline{K_2}$	$\overline{B_1}$	$\overline{B_2}$	$\overline{B_3}$	$\overline{N_1}$	$\overline{N_2}$	$\overline{N_3}$	$\overline{N_4}$
SL	1	1	1	1	1	0	0	0	0

With this the CLP will for the first time detect that the key has been released.

6. Key Coder Output Timing Chart

1. When two sounds are pressed successively within the same octave.

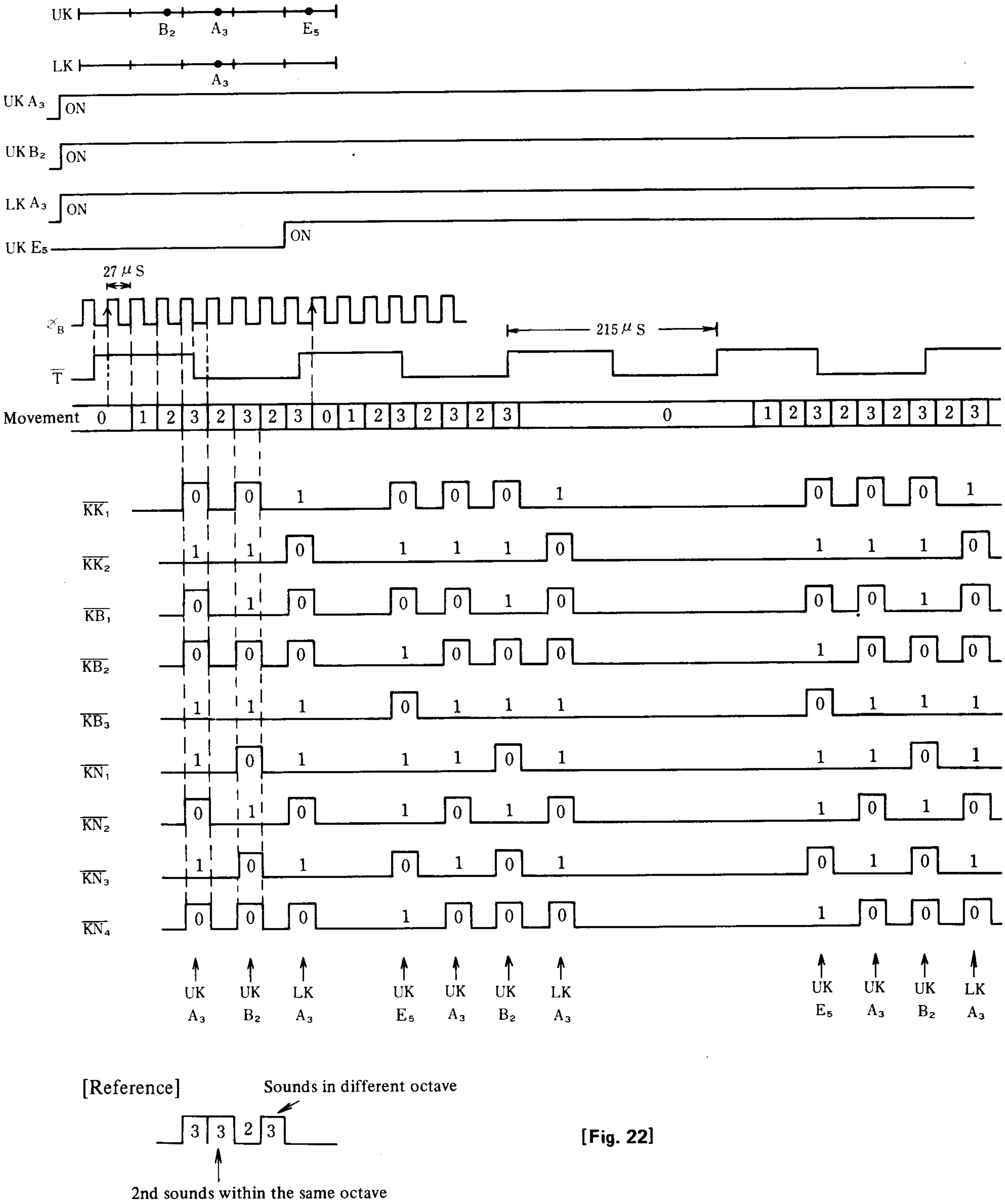


[Fig. 21]

(Reference)

- There is a control counter within the IC to push forward the coding action when the timing (waiting condition) is at 0 and moreover when $\overline{T}$ has risen.
- There is a priority gate circuit within the IC to determine the order of priority for the output.
- When the key is released the key code output will stop at that point but the SL data will output when the timing is at "0" after the 8th rise of the $\overline{T}$ clock, from the last output.

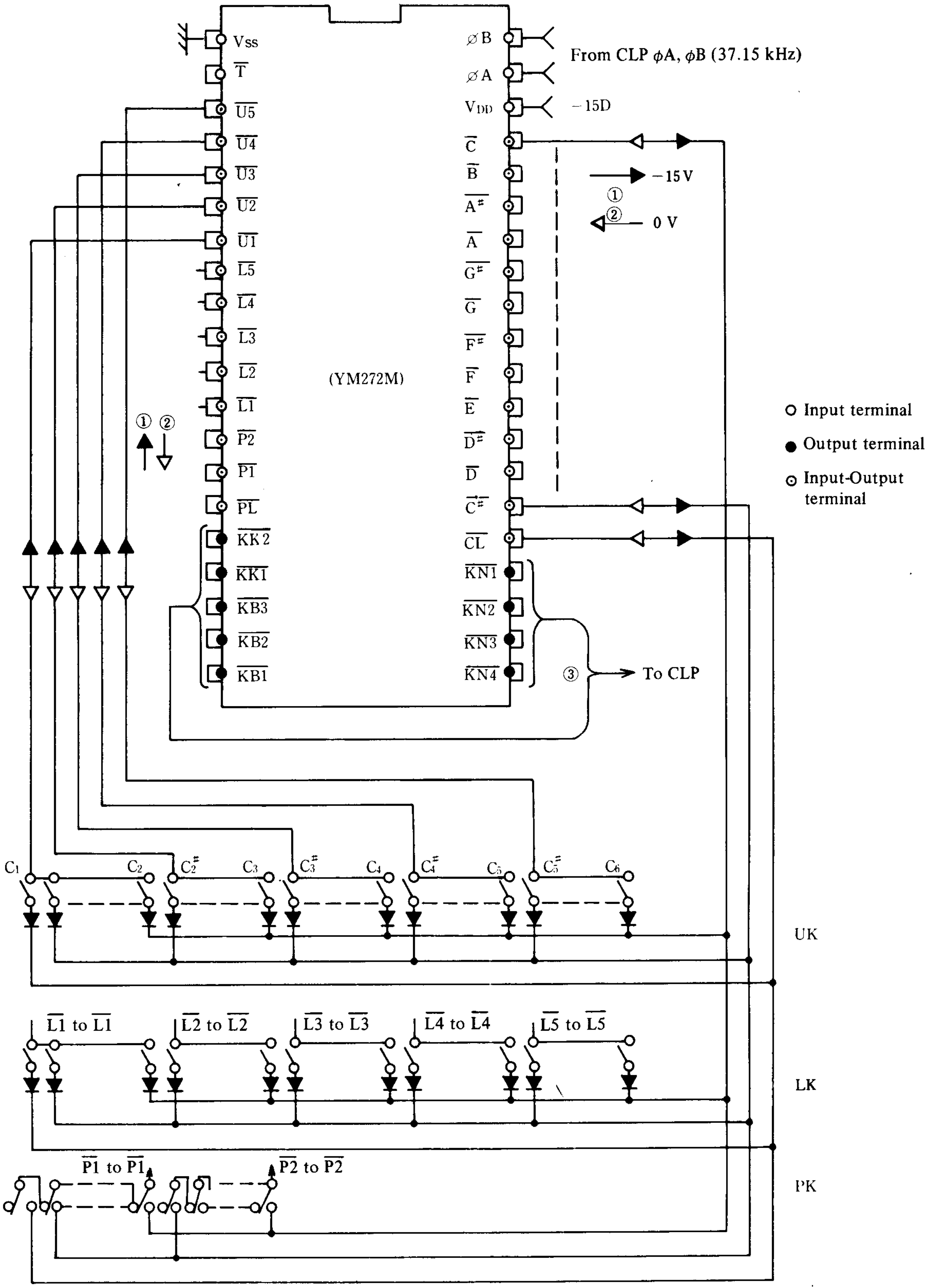
2. When 3 sounds, each of a different octave, are pressed and then a further sound of a different octave is pressed.



[Fig. 22]

7. Wiring Diagram between Keyboard and K · C

[Fig. 23]

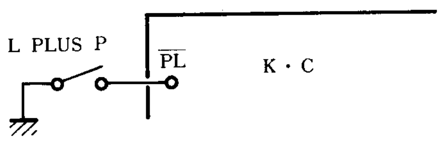


8. $\overline{PL}$ Terminal Operation (Lower Plus Pedal Effect)

Normally, there is −15V present in $\overline{PL}$ terminal of the IC, but when 0V is fed in the PK key code data will be generated with the $C_1 \sim C_2$ key of the LK.

That is, with the $\overline{PL}$ terminal at 0V and when any of the $C_1 \sim C_2$ of LK is pressed, the keyboard code data ($\overline{K_1}$, $\overline{K_2}$) for the highest interval sound among the LKs pressed will change alternately from LK data to PK data.

Therefore, when this $\overline{PL}$ terminal is changed to 0V it will be possible to produce a PK sound at the same time by pressing a LK key. Moreover, at this time there will be no detection of PK switching in the IC, and so, when the PK is pressed there will be no sound.



[Fig. 24]

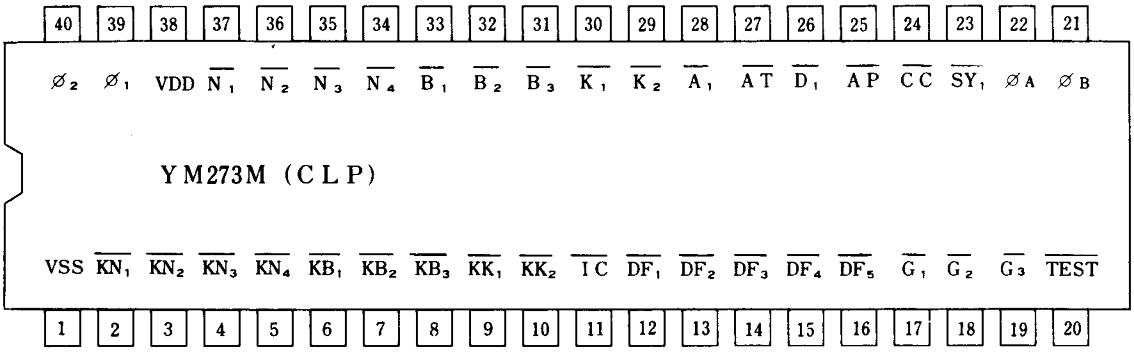
2 — 2 ● CHANNEL PROCESSOR (CLP)

1. CLP Points

A maximum of 12 sounds (11 MK sounds and 1 PK sound) can be received in the order the key code data is pressed from the K·C. From these data various kinds of keyboard information signals are prepared to instruct the production of the sound.

- With this circuit control the simultaneous maximum number of sounds will be 12.
- Explanation of the YM273M (CLP) terminal.

2. YM273M (Channel Processor) Terminal Explanation



Terminal №.	Terminal Code	Designation	Significance	Terminal №.	Terminal Code	Designation	Significance
1	Vss	———	Power source (0V)	40	Ø2	———	Master clock f ≒ 891.6 kHz (ϕ_1 is opposite phase from ϕ_2.)
2	$\overline{KN}_1$	KEY CODER NOTE DATA1	Note data input (4 bits)	39	Ø1	———	
3	$\overline{KN}_2$	〃 2		38	V_{DD}	———	Power source (−15V)
4	$\overline{KN}_3$	〃 3		37	$\overline{N}_1$	NOTE DATA1	Key address data output (7 bits)
5	$\overline{KN}_4$	〃 4		36	$\overline{N}_2$	〃 2	
6	$\overline{KB}_1$	KEY CODER BLOCK DATA1	Block data input (3 bits)	35	$\overline{N}_3$	〃 3	
7	$\overline{KB}_2$	〃 2		34	$\overline{N}_4$	〃 4	
8	$\overline{KB}_3$	〃 3		33	$\overline{B}_1$	BLOCK DATA 1	
9	$\overline{KK}_1$	KEY CODER KEY DATA1	Keyboard data input (2 bits)	32	$\overline{B}_2$	〃 2	
10	$\overline{KK}_2$	〃 2		31	$\overline{B}_3$	〃 3	
11	$\overline{IC}$	INITIAL CLEAR	Counter S/R cleared with power on.	30	$\overline{K}_1$	KEY DATA 1	Keyboard data output (2 bits)
12	$\overline{DF}_1$	DECAY FINISH 1	Data on ending decay	29	$\overline{K}_2$	〃 2	
13	$\overline{DF}_2$	〃 2	〃	28	$\overline{A}_1$	———	Channel occupied data output
14	$\overline{DF}_3$	〃 3	〃	27	$\overline{AT}$	———	KEY-ON data output
15	$\overline{DF}_4$	〃 4	〃	26	$\overline{D}_1$	———	Decay data output (KEY-OFF data)
16	$\overline{DF}_5$	〃 5	〃	25	$\overline{AP}$	ATTACK PULSE	One pulse with KEY-ON
17	$\overline{G}_1$	———	Detects speedy decay from EG (TRUNCATE)	24	$\overline{CC}$	COUNTER CLEAR	Clears the counter of other IC's
18	$\overline{G}_2$	———		23	$\overline{SY}_1$	SYNCHRO 1	Check point terminal (indicating one channel)
19	$\overline{G}_3$	———		22	ØA	———	Clock f = 1/24ϕ_1 — Supplies to KC, ABC
20	TEST	———	Clears the counter and tests (−15V fixed)	21	ØB	———	(opposite phase from ϕA)

[Fig. 25]

3. Principles of Movement

- **Key code data processing**

The key code data successively sent from the K·C is received by the CLP up to a maximum of 12 notes in the order the key is pressed and memorized. Each key code data which has been memorized is output in order, timed at clock ϕ ($\doteqdot$ 1μS) (This timing is referred to as channel time).

Also, each key code data received and memorized by the CLP is circulated within the IC and after 12μS is again output.

Therefore, the key code data which has once been received and memorized is output at regular intervals (12μS frequency) regardless of the input timing of similar data repeatedly sent in from the K·C. With this, this data is memorized every 12μS. This movement of the CLP will be explained taking Channel 12 of TV as an example.

By turning each channel at an interval of 1μS successively, from Channel 1 to Channel 12, the screen (key code data) will change with each 1μS. That is, each respective screen will appear (output) only during the time of the channel.

In this way, as the channels are turned one channel at a time repeatedly, the same picture screen will appear every 12μS as long as there is a broadcast (the key is being pressed). Of course, for channels where there is no broadcast (key is not pressed) no picture will appear.

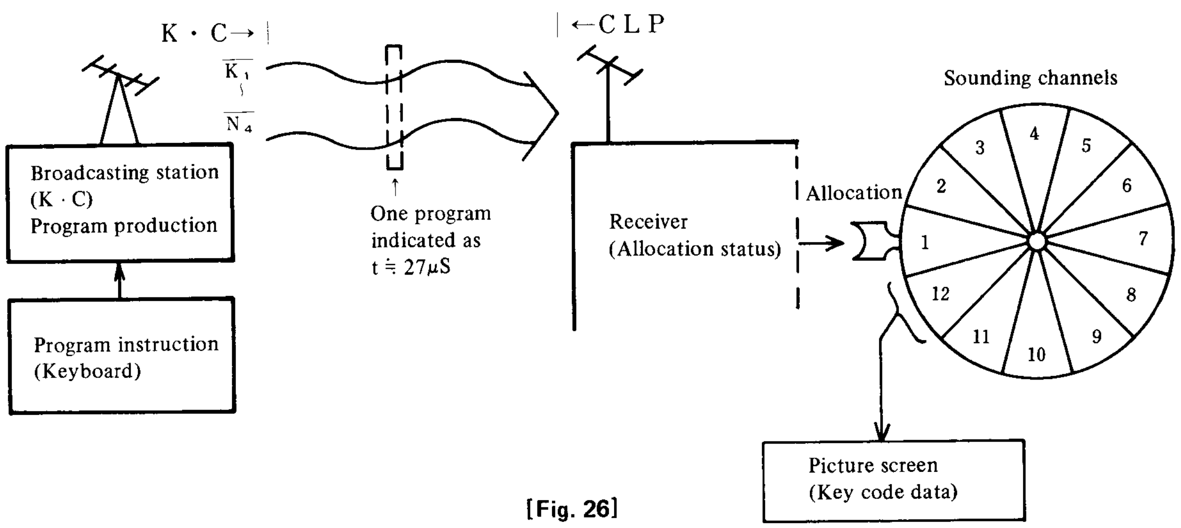
In this way, the CLP has 12 channels for receiving, memorizing and repeated output in succession of key code data for 12 notes. Moreover, the determination of which channel of the 12 channels will be allocated for which key code data will depend on the following conditions within the IC of the CLP.

- **Allocation Status**

(1) The 1st channel is allocated exclusively to the key code data of PK.

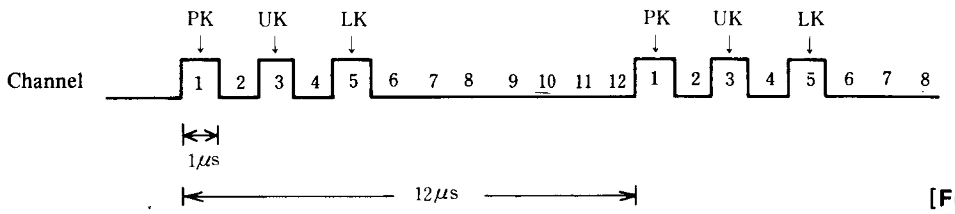
(2) The 2nd channel to the 12th channel are channels exclusively for manual keys (in the order the keys are pressed) with allocation made first for every odd number followed by even numbered channels, such as 3rd channel → 5th channel, → 11th channel → 12th channel → 4th channel .... 12th channel. (to prevent overlapping of the data)

(3) Only one key code data is allocated for the same single channel.



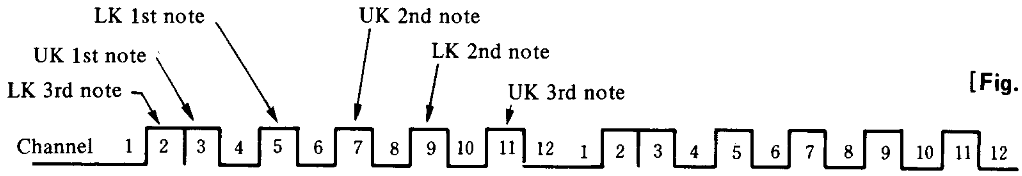
[Fig. 26]

(Example 1) The channel used when UK, LK, and PK are pressed in order one sound at a time.



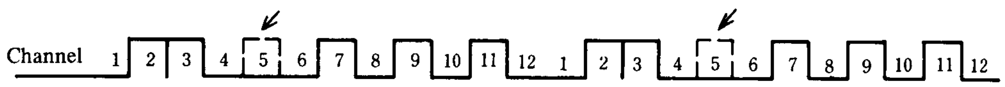
[Fig. 27]

(Example 2) The channel used when the UK and LK are pressed by turns 6 notes at a time.



[Fig. 28]

(Example 3) When the key for the 2nd note of the UK is released in Example 2, the channel is cleared.
(Moreover, the key data of the key depressed after the channel is cleared allocated to the 5th channel.)



[Fig. 29]

4. Key Address Data (Interval Frequency Instruction Data)

- From the output key code data of this CLP, the octave code data ($\overline{B_1} \sim \overline{B_3}$) and the note code data ($\overline{N_1} \sim \overline{N_4}$) are sent to the frequency data generating circuit (to be explained later), to produce the key interval indicated by the interval frequency instruction data (instructions to produce the interval frequency corresponding to the key pressed), and the combination of their code.
- On the other hand, the keyboard data ($\overline{K_1} \sim \overline{K_2}$) are added to the distributor (explained later), which is necessary for determining which keyboard key was pressed, and the generated sound is divided by keyboard.
- In other words, when generating the sound, the interval soud which has been produced can be divided by keyboard, regardless of the keyboard and so among the key code data the octave data and note data are added to the tone signal generation circuit.

Moreover, with the CLP the following actions will take place according to how the keyboard is pressed.

- **KEY-ON AGAIN**

  When the same key is pressed again while the sound is decaying, this function is activated to bring the sound back to the first rise.

  The decaying data ($\overline{D_1}$) is detected inside the IC of the CLP, and when the same note as this data is input by the key coder, one $\overline{CC}$ and one $\overline{AP}$ is sent out and reallocated to the same channel; the sound then generates from the start.

- **TRUNCATE**

When 11 channels for MK are all occupied (11 MK sounds generating) and one is decaying, pressing the 12th MK will detect and clear the channel that is decaying the fastest, and forcefully feed the data of the 12th MK pressed into that channel.

This decaying state is constantly detected within the IC of the CLP receiving the decaying condition data from the EG (envelope generator), through the $\overline{G_1} \sim \overline{G_3}$ terminals.

5. Sound Generation Control Data

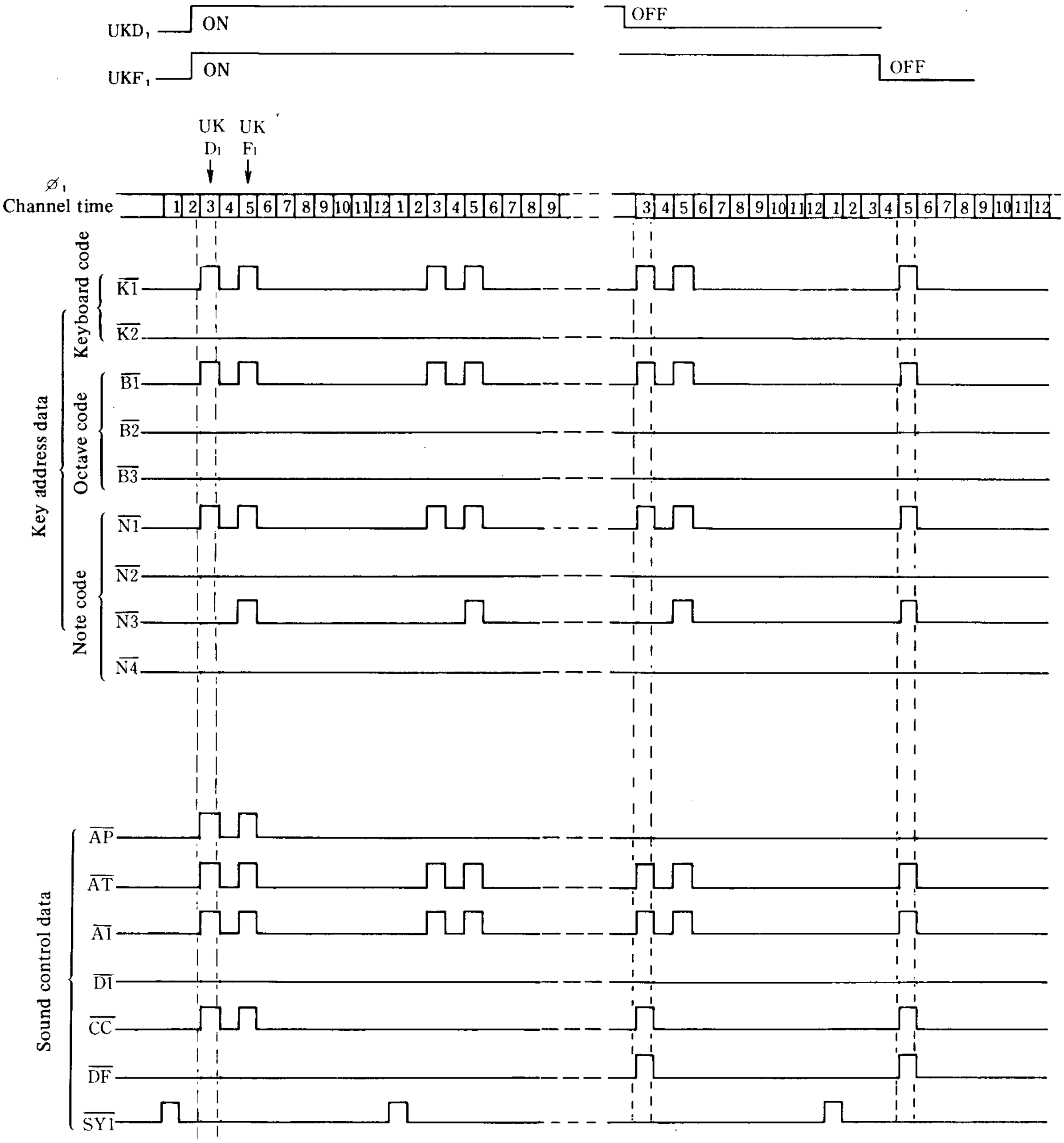
The CLP synchronizes and detects the following kinds of information, instructing the sound generation condition such as start, end, and envelope of the generated sound corresponding to the above-mentioned interval frequency instruction data ($\overline{B_1} \sim \overline{N_4}$).

- **AP (Attack pulse)**
  - (1) When the key is pressed, a single pulse is output, synchronized to the output of the interval frequency instruction data corresponding to that key.
  - (2) With this the percussive mode of the EG (envelope generator) is driven.
- **$\overline{AT}$ (Key-on data)**
  - (1) During the time the key is being pressed a continuous pulse is sent, synchronizing with the output of the interval frequency data corresponding to that key.
  - (2) With this the RD (rhythm driver – explained later) is driven and the rhythm sound generator controlled.
- **$\overline{A_1}$ (Occupied channel data)** **Note: This differs from the A_1 signal of the VG, TVM, ROM, and WC terminals.**
  - (1) The pulse continues to be sent out synchronized to the output of the interval frequency data, corresponding to the key which is generating from the key-on to the end of the decay (memory clear).
  - (2) With this the generating channel occupation is indicated and added to MCA, etc. (explained later)
- **$\overline{D_1}$ (Decay data)**
  - (1) The pulse continues while synchronized to the interval frequency corresponding to that key, from key-off to end of the decay.
  - (2) With this the decay clock is read from the EG (envelope generator – explained later).
- **$\overline{CC}$ (Counter clear)**
  - (1) At the time off key-on (including the truncator action and the time of key-on again), as well as when the decay ends, a single pulse is output, synchronized to the interval frequency data corresponding to that key.
  - (2) With this the ICs for the WC (wave counter) and EG (envelope generator – explained later) are cleared and all return to the original condition.
- **$\overline{DF}$ (Decay end data)**
  - (1) This information inputs a single pulse at the time of the decay end, with the data input from the EG (envelope generator).
  - (2) With this input pulse the $\overline{CC}$ is produced within the IC of the CLP.
- **$\overline{SY_1}$ (Synchro I. . . . . Single channel check data)**
  - (1) Of the channels having a time position a pulse is continuously sent out, synchronized to the 1st channel in which the PK data is entered.
  - (2) By synchronizing with this data it can be determined to which channel the data of the key pressed is sent.

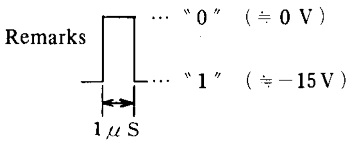
Moreover, the keyboard data ($\overline{K_1}$, $\overline{K_2}$) also has the function of driving the sound envelope. Added to the EG this is used as command data for the direct keying mode.

6. CLP Output Timing Chart

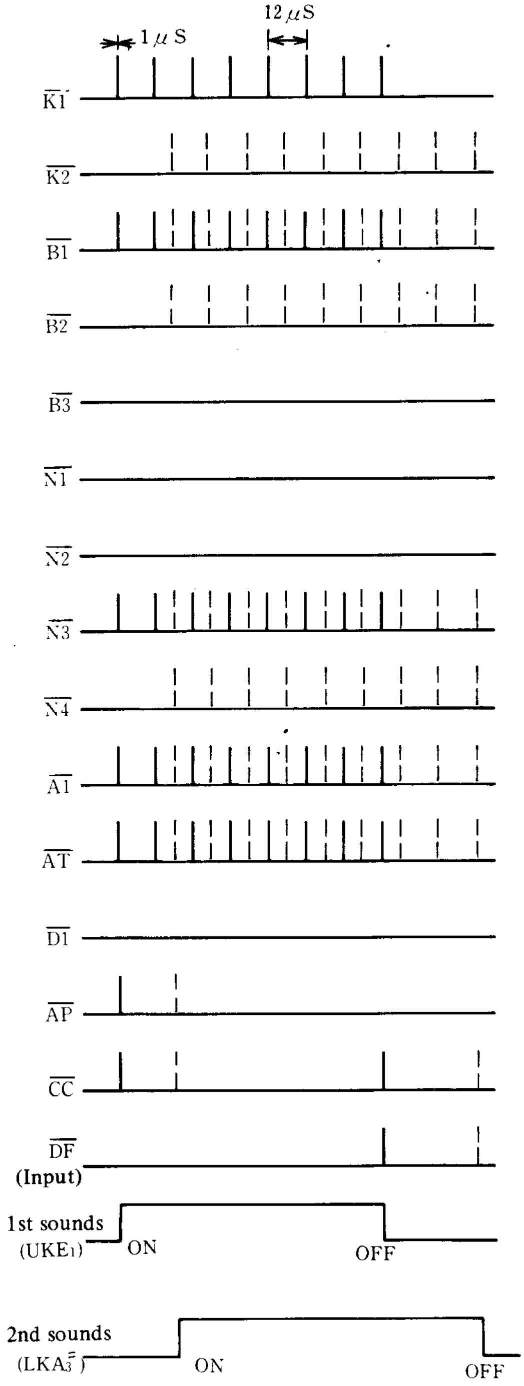
(1) Without SUSTAIN



[Fig. 30]

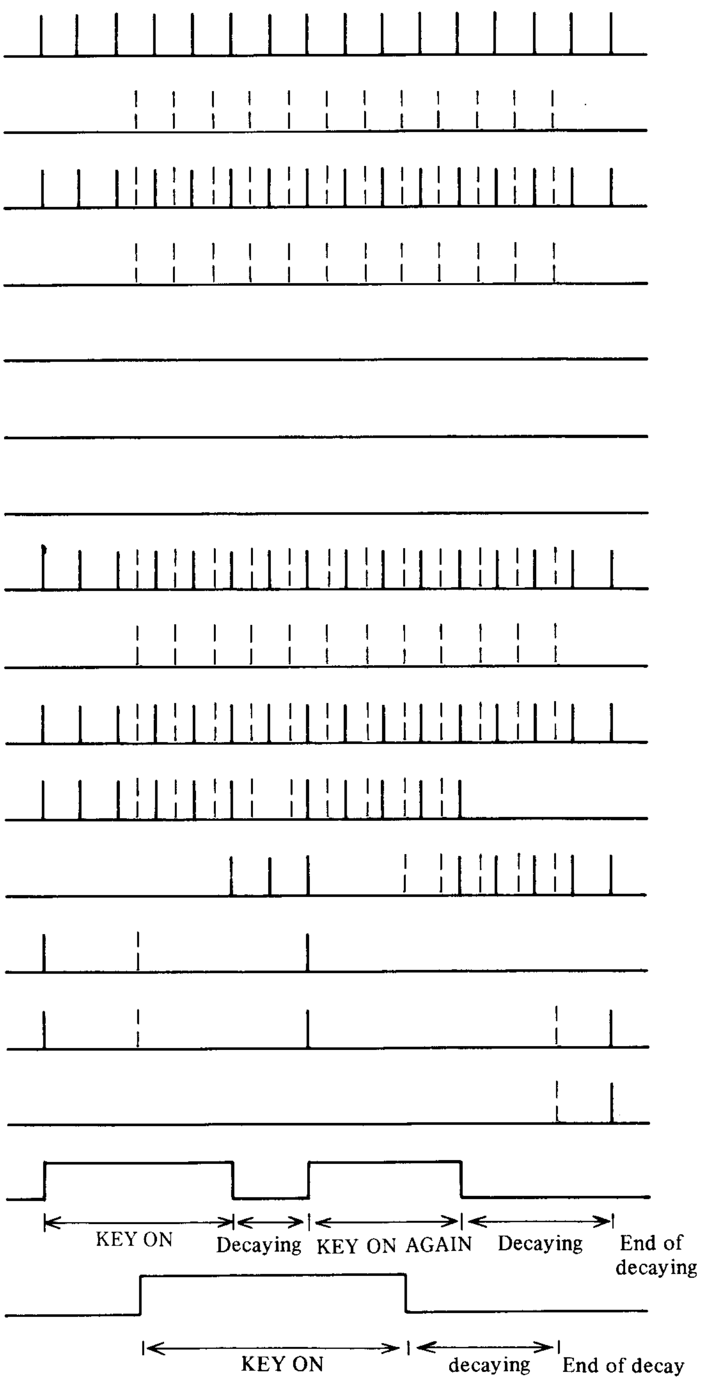


Without SUSTAIN



[Fig. 31]

With SUSTAIN

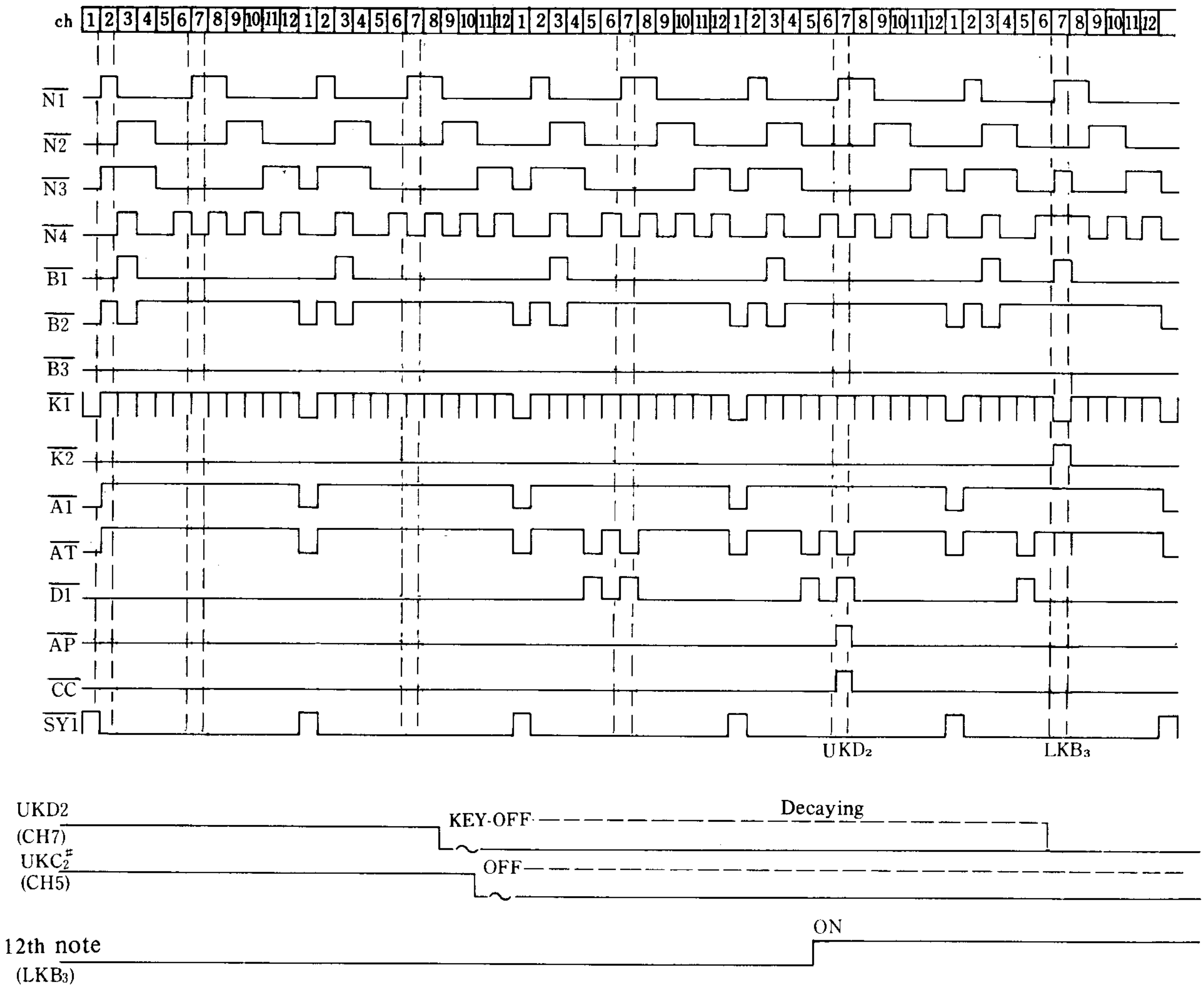


(Remarks) | Line enters CH3 UKE_1
. Line enters CH5 $LKA_3^{\#}$

[Fig. 32]

(3) TRUNCATE

Press 11 notes in order from C_2 to $A_2^{\#}$ on the UK. Then release D_2, $C_2^{\#}$ in order. Then as the 12th note, press LKB_3.

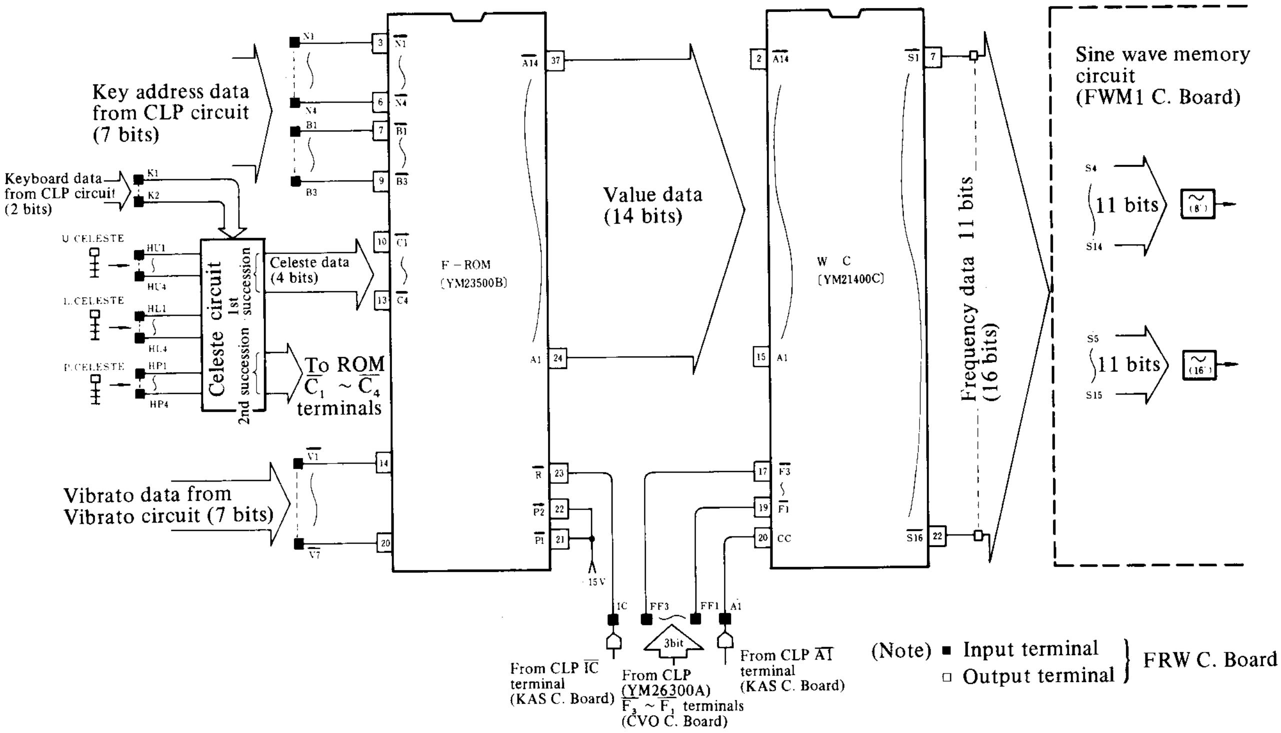


[Fig. 33]

3 ● FREQUENCY DATA GENERATION CIRCUIT [PAS — VCF FOR FLUTE TONE]

○ The frequency data generation circuit produces data (frequency data) to read the memorized wave patterns of the sine wave memory circuit (explained later), through intervals matched to the keys.

○ This frequency data digitally prepares the frequency data of the key intervals indicated by the address data using the key address data ($\overline{B_1}, \overline{B_2}, \overline{B_3}, \overline{N_1}, \overline{N_2}, \overline{N_3}, \overline{N_4}$) sent in by channel from the keyboard data generating circuit.



(Basic construction of the frequency generation circuit I on E-70)

○ Basic Circuit Construction

(1) Frequency Read Only Memory [F–ROM]
The individual tone frequency data of keys $C_1 \sim C_6$ are memorized.

(2) Wave Counter (W · C)
The ROM values are computed and frequency data prepared.
Two kinds of IC's are used. Also has several functions regarding the wave pitch Vibrato, Celeste and Glide.

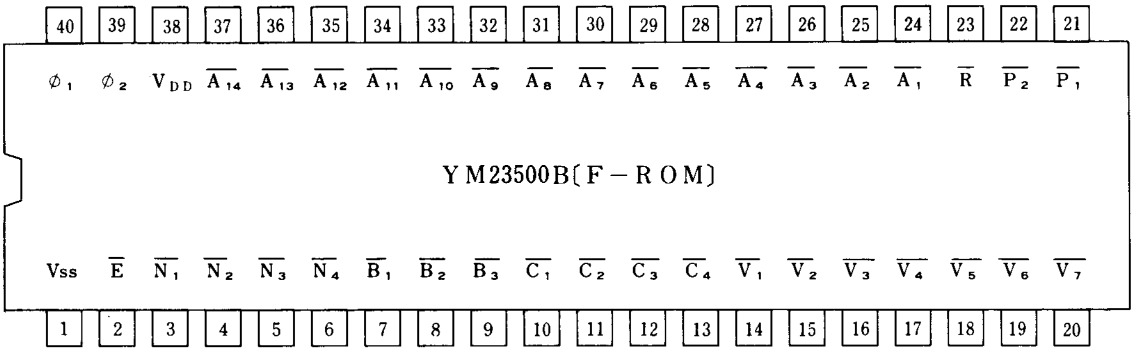
FREQUENCY — READ ONLY MEMORY [F — ROM]

1. Point

The value data corresponding to the interval frequency of each key ($C_1 \sim C_6$) is memorized inside the IC of the F–ROM.

This value data are fed out to WAVE COUNTER (explained later) where they are computed to produce the memorized wave pattern.

2. Explanation of the Terminals for YM23500B (F–ROM)

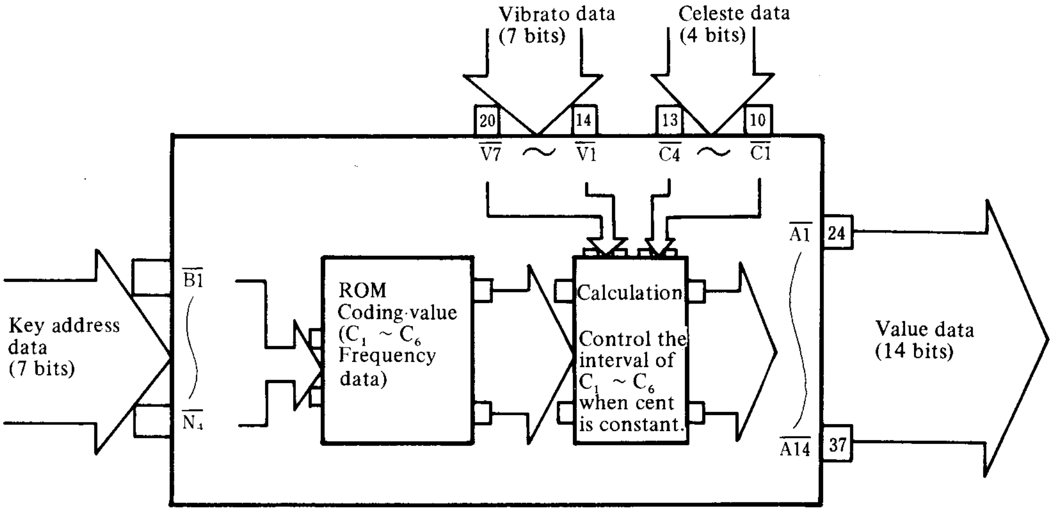


Terminal No.	Terminal Code	Designation	Significance	Terminal No.	Terminal Code	Designation	Significance
1	Vss	———	Power source (0V)	40	$\varnothing_1$	Master clock	f ≒ 891 kHz ϕ_2 is opposite phase from ϕ_1.
2	$\overline{E}$	ENABLE	IC control (0V fixed)	39	$\varnothing_2$	〃	
3	$\overline{N_1}$	NOTE DATA1	Key address data input terminals (7 bits)	38	V_{DD}	———	Power source (−15V)
4	$\overline{N_2}$	〃 2		37	$\overline{A_{14}}$	———	Frequency value data output terminal (14 bits)
5	$\overline{N_3}$	〃 3		36	$\overline{A_{13}}$	———	
6	$\overline{N_4}$	〃 4		35	$\overline{A_{12}}$	———	
7	$\overline{B_1}$	BLOCK DATA1		34	$\overline{A_{11}}$	———	
8	$\overline{B_2}$	〃 2		33	$\overline{A_{10}}$	———	
9	$\overline{B_3}$	〃 3		32	$\overline{A_9}$	———	
10	$\overline{C_1}$	CENT1	Celeste data input terminals (4 bits) (Interval changed at fixed cent.)	31	$\overline{A_8}$	———	
11	$\overline{C_2}$	〃 2		30	$\overline{A_7}$	———	
12	$\overline{C_3}$	〃 3		29	$\overline{A_6}$	———	
13	$\overline{C_4}$	〃 4		28	$\overline{A_5}$	———	
14	$\overline{V_1}$	VIBRATO1	Vibrato terminals input terminals (7 bits) (Interval changed at fixed cent.)	27	$\overline{A_4}$	———	
15	$\overline{V_2}$	〃 2		26	$\overline{A_3}$	———	
16	$\overline{V_3}$	〃 3		25	$\overline{A_2}$	———	
17	$\overline{V_4}$	〃 4		24	$\overline{A_1}$	———	
18	$\overline{V_5}$	〃 5		23	$\overline{R}$	RESET	Memory clear (Matching of timing when ROM is 2 in order.)
19	$\overline{V_6}$	〃 6		22	$\overline{P_2}$	PITCH	Tone changed at fixed pitch (−15V fixed = not used)
20	$\overline{V_7}$	〃 7		21	$\overline{P_1}$	〃	

[Fig. 34]

3. Principle of Movement

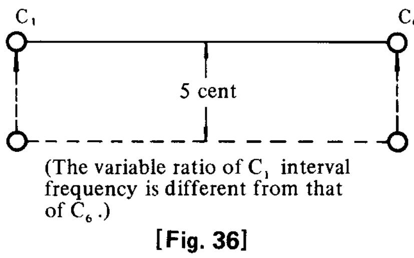
- The value data of 61 notes ($C_1 \sim C_6$) are coded and memorized in F–ROM. The Fig-41 on page 31 shows the frequency data of all tones corresponding to the keys. (ROM coding values) These values are read out by key address data ($\overline{N_1} \sim \overline{B_3}$: 7 bits) fed into from CLP. Since the key address data represent the key (note) name depressed, the value data of the frequencies are read out according to the notes indicating the input address data.
  Moreover, the key address data are repeatedly input into ROM through 12-note time sharing of CLP every 1μS and periodically 12μS (12 channels). Therefore, the coding value memorized inside of ROM IC are repeatedly read out every 12μS in accordance with the above movement.
- In this manner, the value read out by key address data are, further, synchronized with the address data of each channel and calculated by pitch control data (vibrato data: $\overline{V_1} \sim \overline{V_7}$, Celeste Data: $\overline{C_1} \sim \overline{C_4}$) added to ROM to produce the final ROM IC output value data ($\overline{A_1} \sim \overline{A_{14}}$: 14 bits).



[Fig. 35] Block Diagram of F–ROM IC

- The ROM coding values, basic values to produce frequencies of each $C_1 \sim C_6$ key, are memorized as 14 bits code.
- The pitch control values as shown in the above figure are added to ROM coding values and calculated to produce ROM output value data having an uniform change of $C_1 \sim C_6$ interval frequencies with fixed cent.

(Example) Pitch is raised when 5 cent is fixed.



[Fig. 36]

(Note) **Value data of each key memorized within ROM IC are coded with values that are slightly shifted from the equal temperament.**
Therefore, all the notes from C_1 to C_6 produced by ROM coding values are shifted uniformly with a same cent and consequently, they are not shifted with same cent against the equal temperament. (for details, refer to page 37.)

4. The Vibrato Terminals ($\overline{V_1} \sim \overline{V_7}$) and the Celeste Terminals ($\overline{C_1} \sim \overline{C_4}$)

As the value data output $\overline{A_1} \sim \overline{A_{14}}$ terminals of this ROM IC determines the interval frequency of each key, it will be possible to change the intervals by changing the value of the code combinations of these 14 bits. Among the ICs (YM23500) of ROM, the input data of the vibrato terminals ($\overline{V_1} \sim \overline{V_7}$), as well as the celeste terminals ($\overline{C_1} \sim \overline{C_4}$) and the pitch terminals ($\overline{P_1}, \overline{P_2}$), are used to change the original memory and the interval.

- **Vibrato Terminals ($\overline{V_1} \sim \overline{V_7}$)**

With this vibrato terminal input data, the output data of the ROM is changed, and as a result the intervals over the entire range of the keyboard receive this change in the same number of cents.

When each terminal for the 6 bits from $\overline{V_1} \sim \overline{V_6}$ is changed from "1" (no change in the frequency of the vibrato) to "0" the interval frequency changes for each are expressed as shown below.

Vibrato terminal	$\overline{V_1}$	$\overline{V_2}$	$\overline{V_3}$	$\overline{V_4}$	$\overline{V_5}$	$\overline{V_6}$	$\overline{V_7}$
Interval frequency change	1.6	3.2	6.4	12.8	25.6	51.2	※

(Unit: Cent)

[Fig. 37]

(Note)
When $\overline{V_7}$ is at "1" the frequency changes of the vibrato will be in the high (plus) direction of the original interval and when at "0" will be in the low (minus) direction.

Also, $\overline{V_7}$ decides whether the changes in frequency from $\overline{V_1} \sim \overline{V_7}$ will change in the plus direction or in the minus direction compared to the original interval.

(Example) **[Fig. 38]**

Vibrato terminals							Interval frequency change	
$\overline{V_1}$	$\overline{V_2}$	$\overline{V_3}$	$\overline{V_4}$	$\overline{V_5}$	$\overline{V_6}$	$\overline{V_7}$		
0	0	0	0	0	0	0	−100.8 cent	⇨ Glide
1	1	1	1	1	1	1	0 cent	⇨ at Normal

When Glide effect is taken, foot switch ON gives "0" to all V terminals.
Also, in order to obtain the vibrato effect, data of $\overline{V_1} \sim \overline{V_7}$ are changed periodically.

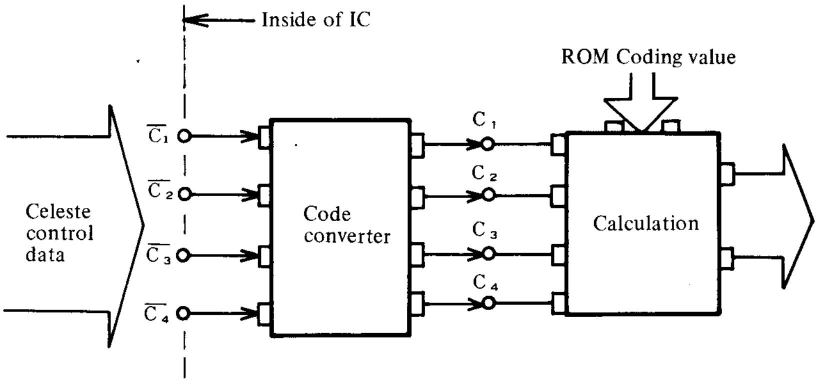
(Reference)
The 7 bits code data, changed 5 – 7 Hz with the VG (vibrato generator) activated by the Vibrato/Glide/Attack Pitch lever, is input into the vibrato terminal through time division and synchronized to the address data of each key. Therefore, each key will receive the vibrato effect which changes in interval periodically with the vibrato lever. When the panel levers are at Off, all the vibrato terminals become "1" and there is no interval changes.

- **Celeste Terminal ($\overline{C_1} \sim \overline{C_4}$)**

Like the vibrato, interval of each key is changed in a fixed cent number uniformly by this celeste terminal input data (4 bits).

The values of varying intervals depend on the combination of 4-bit code added to $\overline{C_1} \sim \overline{C_4}$ terminals.

The IC (YM23500) of ROM converts the data added to celeste terminals $\overline{C_1} \sim \overline{C_4}$ into code and determines the intervals and the value of varying.



[Fig. 39]

4-bit code data are input into the celeste terminals $\overline{C_1} \sim \overline{C_4}$ by channel by time sharing with the control of each lever for UK, LK and PK on the panel.

These data, even though the levers are all in normal position (OFF position), can be changed in accordance with keyboards by depressing respective keys.

Celeste lever (All in normal position)	IC terminals of ROM				Code conversion within IC			
	$\overline{C_1}$	$\overline{C_2}$	$\overline{C_3}$	$\overline{C_4}$	C_1	C_2	C_3	C_4
for UK	0	1	0	0	1	0	0	1
for LK	1	1	0	0	0	0	0	1
for PK	1	1	0	1	1	1	1	0

[Fig. 40]

(Note)
The ROM IC converts the data added to $C_1 \sim C_4$ into the code and calculates the ROM coding values read out by the coded data and address data. (for details, refer to celeste circuit.)

Therefore, on PAS–VCF Electone, ROM output values ($\overline{A_1} \sim \overline{A_{14}}$) differ according to the keyboard, even though the celeste levers are all in "Normal" position.

(Reference)

As the tone generating circuit for flute is made up of two systems for the E-70 there are 2 ROMs. Therefore, when different code data are input into the $\overline{C_1} \sim \overline{C_4}$ terminals of the two ROMs, two sounds with differing intervals will be produced, or a celeste effect (same with orchestra).

For the E-50 also, this is made up of a single system tone generation circuit for both the flute and the orchestra, and so by adding celeste data to the ROMs of both, a celeste effect can be obtained.

5. ROM Input-Output Data

(Note: VIBRATO=OFF, CELESTE=NORMAL)

KEY	Key address data input							ROM	Output value		
	B_1	B_2	B_3	N_1	N_2	N_3	N_4	Value	UK	LK	PK
OFF	1	1	1	1	1	1	1	——	0	0	0
C_1	1	1	1	1	0	0	0	458	461	461	459
$C_1^{\#}$	0	1	1	1	1	1	1	486	495	489	487
D_1	0	1	1	0	1	1	1	512	517	516	515
$D_1^{\#}$	0	1	1	1	0	1	1	543	547	547	546
E_1	0	1	1	1	1	0	1	576	580	580	579
F_1	0	1	1	0	1	0	1	611	615	615	614
$F_1^{\#}$	0	1	1	1	0	0	1	647	652	652	650
G_1	0	1	1	1	1	1	0	686	691	690	689
$G_1^{\#}$	0	1	1	0	1	1	0	727	733	732	730
A_1	0	1	1	1	0	1	0	769	775	775	773
$A_1^{\#}$	0	1	1	1	1	0	0	816	822	822	820
B_1	0	1	1	0	1	0	0	865	871	871	869
C_2	0	1	1	1	0	0	0	916	923	923	920
$C_2^{\#}$	1	0	1	1	1	1	1	972	979	979	976
D_2	1	0	1	0	1	1	1	1026	1035	1034	1033
$D_2^{\#}$	1	0	1	1	0	1	1	1088	1097	1096	1096
E_2	1	0	1	1	1	0	1	1155	1163	1162	1161
F_2	1	0	1	0	1	0	1	1223	1233	1232	1231
$F_2^{\#}$	1	0	1	1	0	0	1	1295	1306	1305	1304
G_2	1	0	1	1	1	1	0	1373	1384	1383	1382
$G_2^{\#}$	1	0	1	0	1	1	0	1455	1467	1466	1463
A_2	1	0	1	1	0	1	0	1539	1552	1551	1549
$A_2^{\#}$	1	0	1	1	1	0	0	1632	1645	1644	1642
B_2	1	0	1	0	1	0	0	1730	1744	1743	1740
C_3	1	0	1	1	0	0	0	1832	1847	1846	1843
$C_3^{\#}$	0	0	1	1	1	1	1	1942	1958	1957	
D_3	0	0	1	0	1	1	1	2055	2073	2071	
$D_3^{\#}$	0	0	1	1	0	1	1	2178	2197	2195	
E_3	0	0	1	1	1	0	1	2308	2328	2326	
F_3	0	0	1	0	1	0	1	2447	2468	2466	
$F_3^{\#}$	0	0	1	1	0	0	1	2591	2613	2611	

KEY	Key address data input							ROM	Output value		
	B_1	B_2	B_3	N_1	N_2	N_3	N_4	Value	UK	LK	PK
G_3	0	0	1	1	1	1	0	2746	2769	2767	
$G_3^{\#}$	0	0	1	0	1	1	0	2910	2934	2932	
A_3	0	0	1	1	0	1	0	3081	3108	3105	
$A_3^{\#}$	0	0	1	1	1	0	0	3266	3294	3291	
B_3	0	0	1	0	1	0	0	3460	3490	3487	
C_4	0	0	1	1	0	0	0	3666	3697	3694	
$C_4^{\#}$	1	1	0	1	1	1	1	3884	3917	3914	
D_4	1	1	0	0	1	1	1	4113	4149	4145	
$D_4^{\#}$	1	1	0	1	0	1	1	4359	4397	4393	
E_4	1	1	0	1	1	0	1	4618	4658	4654	
F_4	1	1	0	0	1	0	1	4894	4936	4932	
$F_4^{\#}$	1	1	0	1	0	0	1	5184	5229	5224	
G_4	1	1	0	1	1	1	0	5494	5541	5536	
$G_4^{\#}$	1	1	0	0	1	1	0	5820	5870	5865	
A_4	1	1	0	1	0	1	0	6165	6219	6213	
$A_4^{\#}$	1	1	0	1	1	0	0	6533	6590	6584	
B_5	1	1	0	0	1	0	0	6921	6981	6975	
C_5	1	1	0	1	0	0	0	7333	7397	7390	
$C_5^{\#}$	0	1	0	1	1	1	1	7769	7836	7829	
D_5	0	1	0	0	1	1	1	8230	8302	8294	
$D_5^{\#}$	0	1	0	1	0	1	1	8720	8796	8788	
E_5	0	1	0	1	1	0	1	9238	9319	9310	
F_5	0	1	0	0	1	0	1	9788	9873	9864	
$F_5^{\#}$	0	1	0	1	0	0	1	10370	10461	10451	
G_5	0	1	0	1	1	1	0	10989	11084	11074	
$G_5^{\#}$	0	1	0	0	1	1	0	11640	11741	11730	
A_5	0	1	0	1	0	1	0	12332	12440	12428	
$A_5^{\#}$	0	1	0	1	1	0	0	13067	13181	13169	
B_5	0	1	0	0	1	0	0	13843	13964	13951	
C_6	0	1	0	1	0	0	0	14667	14795	14781	
	$\overline{B_1}$	$\overline{B_2}$	$\overline{B_3}$	$\overline{N_1}$	$\overline{N_2}$	$\overline{N_3}$	$\overline{N_4}$	Value expressed by decimal notation for $\overline{A_1}$ ~ $\overline{A_{14}}$ (14 bits) code data.			

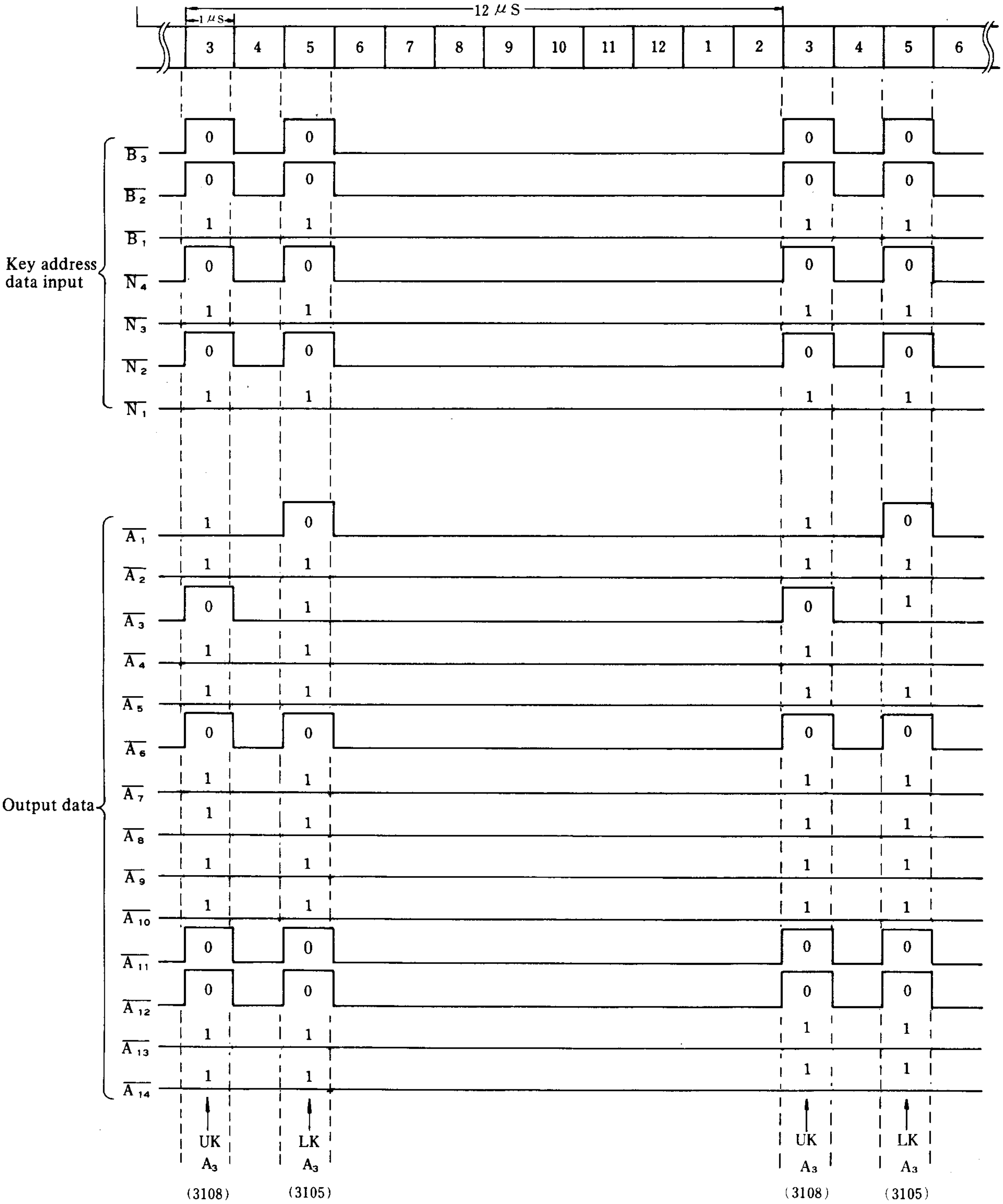
(Reference)

	$\overline{A_1}$	$\overline{A_2}$	$\overline{A_3}$	$\overline{A_4}$	$\overline{A_5}$	$\overline{A_6}$	$\overline{A_7}$	$\overline{A_8}$	$\overline{A_9}$	$\overline{A_{10}}$	$\overline{A_{11}}$	$\overline{A_{12}}$	$\overline{A_{13}}$	$\overline{A_{14}}$
Binary notation	2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}	2^{12}	2^{13}
Decimal notation	1	2	4	8	16	32	64	128	256	512	1024	2048	4096	8192

[Fig. 41]

Example for ROM Input-Output

When the UK A_3 note and the LK A_3 note are pressed the input and output data of the ROM circuit will be as follows: (Celeste lever and vibrato lever are both in OFF position.)



[Fig. 42]

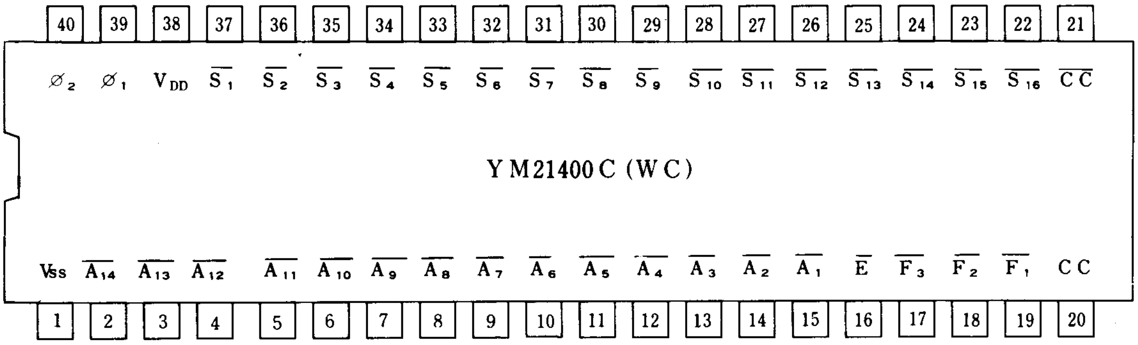
WAVE COUNTER (W · C)

1. Point

The WC successively adds the individual value data coming from the ROM through time sharing to each key, at intervals of 12μS each.

This added effect is used as data (frequency data) to read out the memory wave patterns of the sine wave memory circuit, explained later.

2. Explanation of IC (YM21400C) Terminals



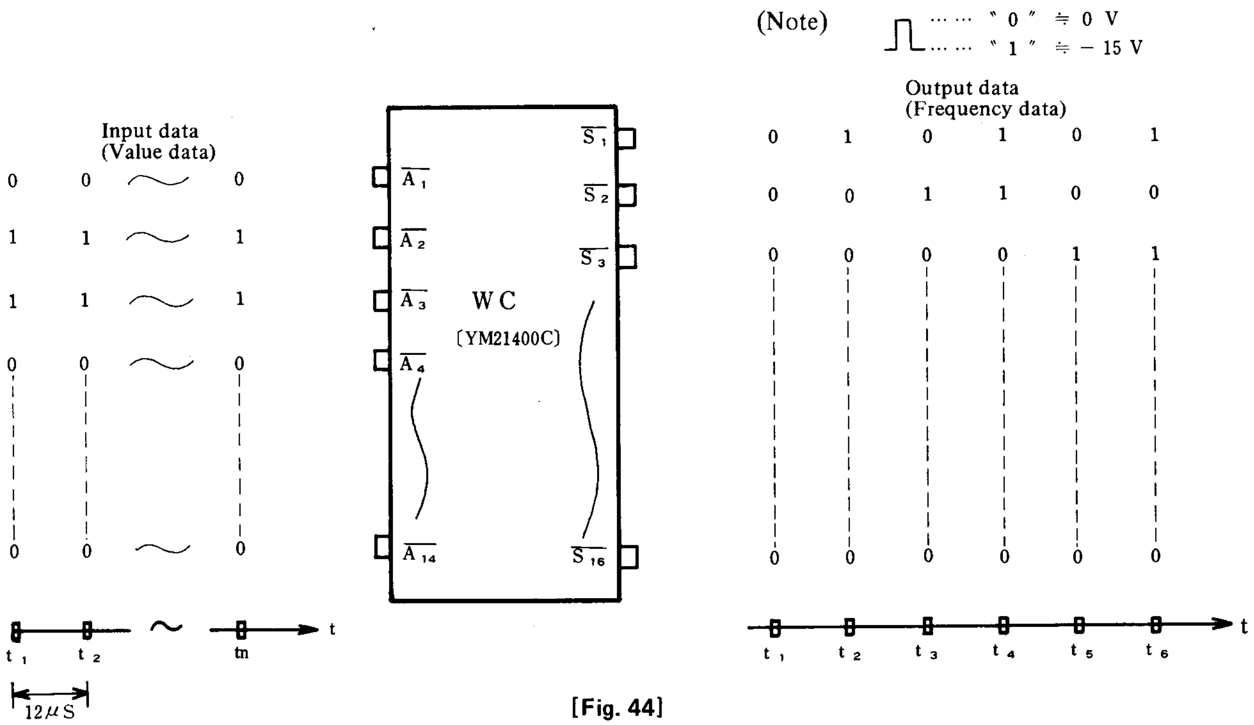
Terminal No.	Terminal Code	Designation	Significance	Terminal No.	Terminal Code	Designation	Significance
1	Vss	————	Power source (0V)	40	$\varnothing_2$	Master clock	f ≒ 891kHz
2	$\overline{A_{14}}$	————		39	$\varnothing_1$	〃	ϕ_2 is opposite phase from ϕ_1.
3	$\overline{A_{13}}$	————		38	V_{DD}	————	Power source (−15V)
4	$\overline{A_{12}}$	————		37	$\overline{S_1}$	————	(2^{13} f)
5	$\overline{A_{11}}$	————		36	$\overline{S_2}$	————	(2^{12} f)
6	$\overline{A_{10}}$	————		35	$\overline{S_3}$	————	(2^{11} f)
7	$\overline{A_9}$	————		34	$\overline{S_4}$	————	(2^{10} f)
8	$\overline{A_8}$	————	Input of frequency value data from ROM. (14 bits)	33	$\overline{S_5}$	————	(2^9 f)
9	$\overline{A_7}$	————		32	$\overline{S_6}$	————	(2^8 f)
10	$\overline{A_6}$	————		31	$\overline{S_7}$	————	(2^7 f)
11	$\overline{A_5}$	————		30	$\overline{S_8}$	————	(2^6 f) Frequency data output (16 bits)
12	$\overline{A_4}$	————		29	$\overline{S_9}$	————	(2^5 f)
13	$\overline{A_3}$	————		28	$\overline{S_{10}}$	————	(2^4 f)
14	$\overline{A_2}$	————		27	$\overline{S_{11}}$	————	(2^3 f)
15	$\overline{A_1}$	————		26	$\overline{S_{12}}$	————	(2^2 f)
16	$\overline{E}$	ENABLE	Controls IC movement 0V fixed.	25	$\overline{S_{13}}$	————	(2^1 f)
17	$\overline{F_3}$	FEET CHANGE		24	$\overline{S_{14}}$	————	(f)
18	$\overline{F_2}$	〃	Feet change octave switching (3 bits)	23	$\overline{S_{15}}$	————	(f/2)
19	$\overline{F_1}$	〃		22	$\overline{S_{16}}$	————	(f /4)
20	CC	COUNTER CLEAR	Input into the $\overline{A_1}$ data from CLP to calculate by channels.	21	$\overline{CC}$	COUNTER CLEAR	−15V fixed

[Fig. 43]

3. Principle of Movement

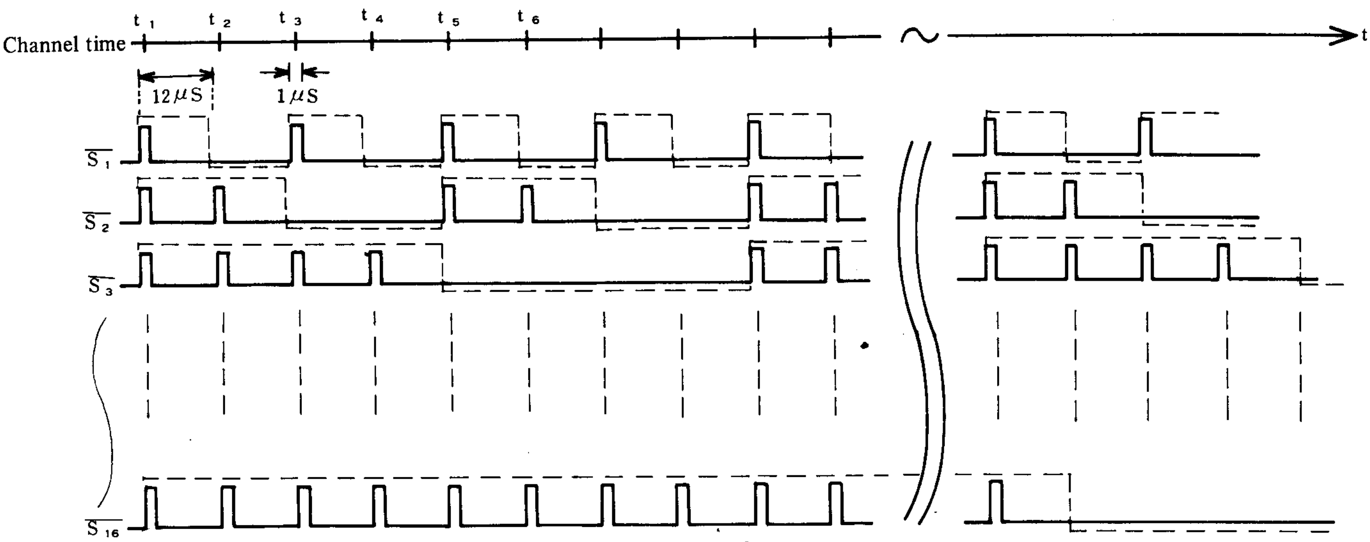
The particular value data of each key depressed are repeatedly sent to WC by channel time from ROM. These 14-bit value data are synchronously computed and output to the terminals $\overline{S_1} \sim \overline{S_{16}}$ as 16-bit code data (frequency data)

(Example) Input-output of WC when a key is depressed.
(Assuming that the key is depressed, data from ROM, namely the value peculiar to the frequency of the depressed, are 0, 1, 1, 0.)



[Fig. 44]

(Output Data Chart)



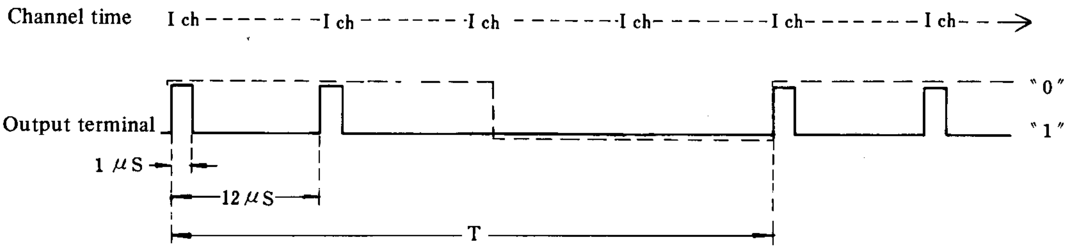
[Fig. 45]

The 'Output Data Chart' shows us the computed results are output with 16-bit code according to the channel time.

Here, as concerns each WC output terminals ($\overline{S_1} \sim \overline{S_{16}}$), we can see that the cumulative results of the WC is "0" pulse synchronized, and a single frequency is formed.

In other words, the WC computes value data sent from the ROM synchronizing with each channel time and output digital data by which the frequency and it's multiples corresponding to the key depressed are formed.

(Example)



Relation between WC output terminal and output frequency data. [Fig. 46]

Output terminal	$\overline{S1}$	$\overline{S2}$	$\overline{S1}$	$\overline{S4}$	$\overline{S5}$	$\overline{S6}$	$\overline{S7}$	$\overline{S8}$	$\overline{S9}$	$\overline{S10}$	$\overline{S11}$	$\overline{S12}$	$\overline{S13}$	$\overline{S14}$	$\overline{S15}$	$\overline{S16}$
Output frequency	2^{13} f	2^{12} f	2^{11} f	2^{10} f	2^{9} f	2^{8} f	2^{7} f	2^{6} f	2^{5} f	2^{4} f	2^{3} f	2^{2} f	2^{1} f	f	$\frac{f}{2}$	$\frac{f}{4}$
Overtone degree	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	Fundamental	½	¼

(Note) Feet change terminals are in NORMAL.

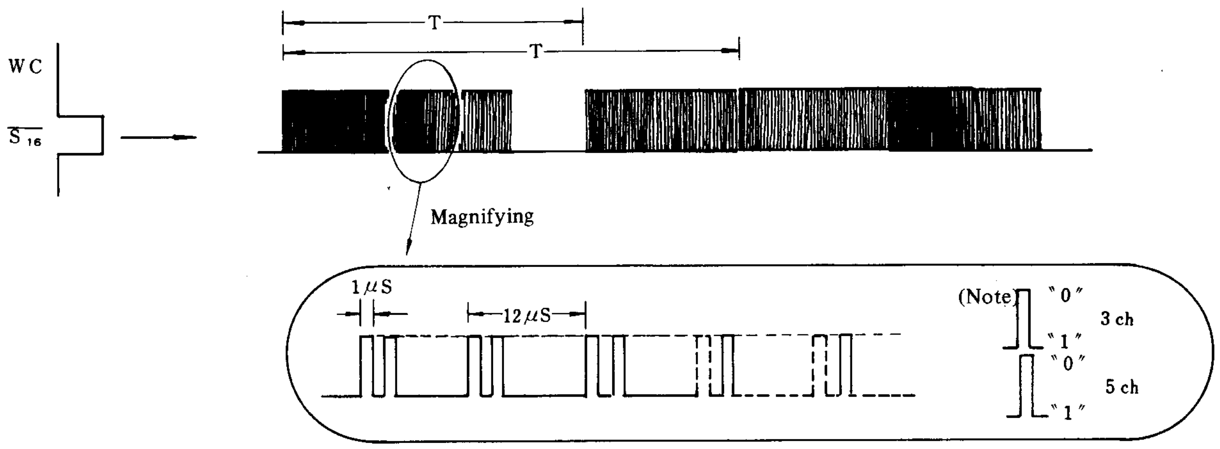
↑ Fundamental (Frequency of the key depressed.)

(Reference) The WC output data, when seen by the synchroscope among others, appears to be a rectangular.

[Fig. 47]

○ Moreover, output is made in succession of the calculations for each channel with the WC, and so when more than two notes are pressed the output frequency appears according to each channel. Therefore, when keys for more than 2 notes are pressed the output small wave patterns for these will appear overlapped. However, as these waves are made from a combination of "0" and "1" by each channel time there will be no collapsing through Mixing.

(Example) WC output when 2 keys are depressed.
(The terminal S_{16} is taken up among others.)

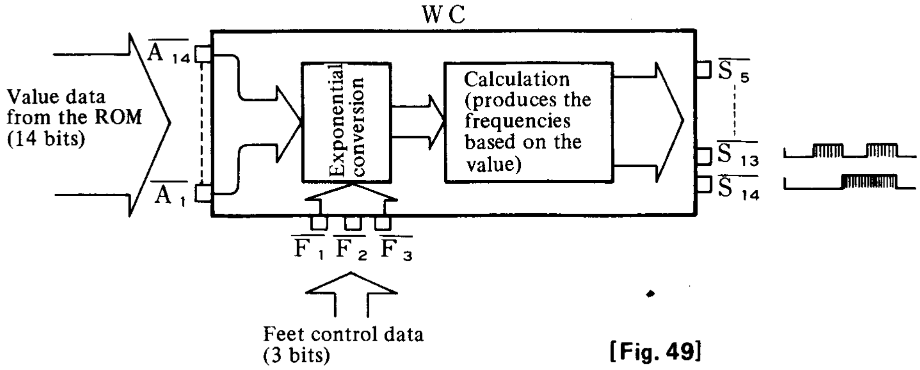


[Fig. 48]

(Reference)
The sound can be heard for the first time with signal checker for the output terminals ($\overline{S_1} \sim \overline{S_{16}}$) of this WC.
However, as the interval sound of the key pressed can be heard at terminal $\overline{S_{14}}$, and the frequency sound related to the overtone can be heard at each terminal, there are terminals which exceed the range of hearing.

4. Feet Change (Octave Switching) Terminals

○ The PAS–VCF Electone carry out the feet change control according to the 3-bit feet control data added to the WC terminals $\overline{F_1} \sim \overline{F_3}$.
In other words, this WC converts the value data ($\overline{A_1} \sim \overline{A_{14}}$: 14 bits) sent from the ROM from ½ times to 4 times (½, 1, 2, 4) exponentially by controlling the mode of the $\overline{F_1} \sim \overline{F_3}$ terminals. The converted values are computed to produce the frequencies corresponding the the key pressed.



[Fig. 49]

Therefore, the frequencies, the data fed out from the WC terminals $\overline{S_1} \sim \overline{S_{16}}$ (16 bits), are controlled by feet control data by octave relation added to the terminals $\overline{F_1} \sim \overline{F_3}$.

Octave switching terminals			Frequencies indicated by output data of terminals $\overline{S_1} \sim \overline{S_{16}}$					Feet change value (octave switching)
$\overline{F_1}$	$\overline{F_2}$	$\overline{F_3}$	$\overline{S_1}$	$\overline{S_2}$	$\overline{S_{14}}$	$\overline{S_{15}}$	$\overline{S_{16}}$	
1	1	1	13 f	12 f	½ f	¼ f	⅛ f	1OCT DOWN
0	1	1	14 f	13 f	f	½ f	¼ f	NORMAL
1	0	1	15 f	14 f	2 f	f	½ f	1OCT UP
0	0	1	16 f	15 f	3 f	2 f	f	2OCT UP
1	1	0	17 f	16 f	4 f	3 f	2 f	3OCT UP

[Fig. 50]

(Note)
The table to the left depends on when the key of frequency f is depressed.

On PAS–VCF Electone, the WC terminals $\overline{F_1} \sim \overline{F_3}$ for Flute family sounds are directly controlled by the Auto Arpeggio circuits. When the effect is in OFF, these terminals are set to the NORMAL condition.

(Reference)
The interval value table is for PAS–VCF Electone is shown as below. The values are comparsion with the equal temperament. When the master clock is adjusted so that the A_3 tone on lower keyboard becomes 440 Hz + 3 cent.

	OCT \ NOTE	C	C#	D	D#	E	F	F#	G	G#	A	A#	B	C
UK	1	1.1	3.2	−3.8	−3.5	−1.4	0.04	1.2	1.7	1.5	0.3	2.2	2.5	
	2	2.9	4.8	1.1	1.8	3.0	4.2	3.7	4.1	5.0	2.5	3.2	4.4	
	3	3.7	4.8	4.6	4.1	4.4	5.5	4.3	4.7	4.9	4.7	5.3	5.4	
	4	5.1	5.2	4.8	5.3	5.1	5.5	5.3	5.6	5.5	5.4	5.8	5.6	
	5	5.8	5.6	5.6	5.7	5.7	5.8	5.7	5.9	5.6	5.8	5.9	5.8	5.9
LK	1	1.1	3.2	−3.8	−2.8	−1.4	0.04	1.2	1.7	1.5	0.3	2.2	2.5	
	2	2.9	4.8	−0.5	0.3	1.5	2.7	2.4	2.9	3.8	1.4	2.1	3.4	
	3	2.8	3.9	1.9	2.6	2.9	4.1	3.0	3.5	3.8	3.0	3.3	3.9	
	4	3.7	3.8	3.1	3.7	3.6	4.1	3.7	4.1	4.0	3.8	4.2	4.1	
	5	4.2	4.1	3.9	4.1	4.0	4.1	4.1	4.4	4.0	4.1	4.8	4.2	4.3
PK	0	−6.4	−3.9	−7.1	−6.0	−4.4	−2.8	−4.1	−3.3	−3.3	−4.1	−2.0	−1.5	
	1	−2.8	−0.5	−2.2	−1.3	−1.5	−0.6	−0.3	0.4	0.2	−0.9	0.1	0.4	0

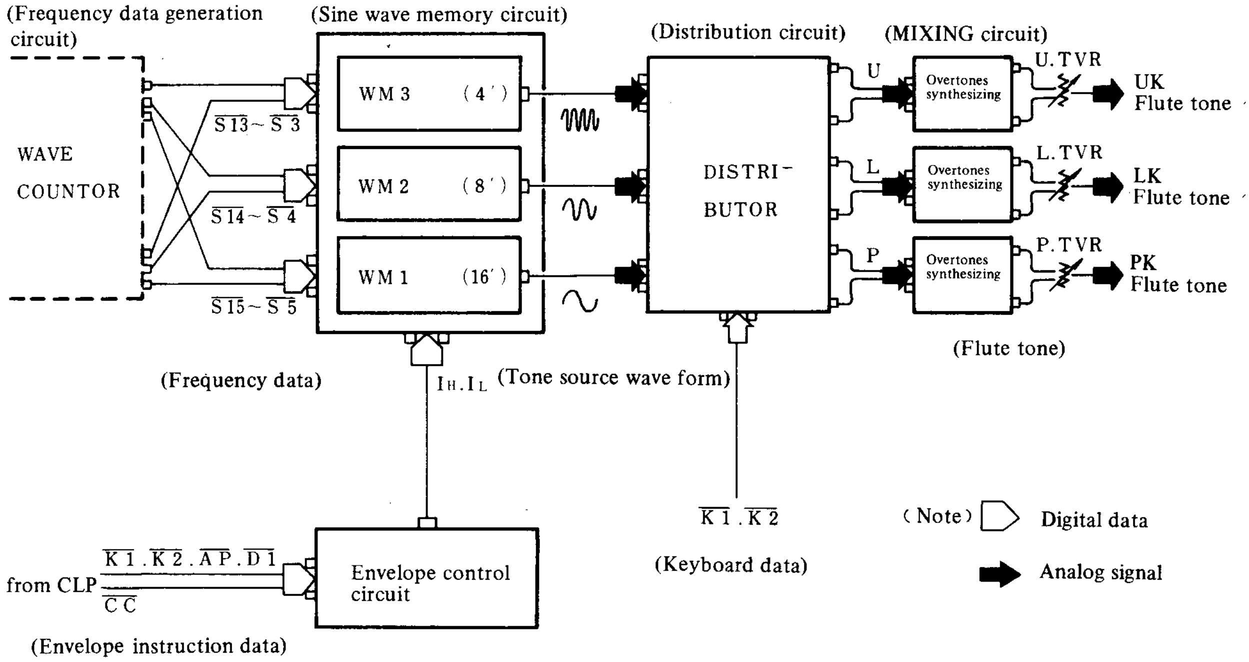
o Celeste lever is in NORMAL position (unit: cent)

[Fig. 51] Interval value of PAS–VCF Electone against the equal temperament.

The WC input data, the different values according to the keyboard even though the similar note key is depressed, are sent from the ROM. The values are used to produce each frequency, therefore, the intervals of them are different from conventional equal temperament by key by keyboard. (Refer to page 31)

4 ● SOUND GENERATION CIRCUIT (PAS SYSTEM)

The Sound Generation Circuit I produces flute-like tones through sine wave synthesizing system. That is, by making use of the frequency data created by beforementioned frequency data generation circuit I, the possible sine wave frequencies related to the overtones are produced simultaneously. Flute-like tones are created by mixing these sine waves of which oscillation width (amplitude) are varied respectively.
(This circuit method is referred to PULSE ANALOG SYNTHESIZING SYSTEM.)



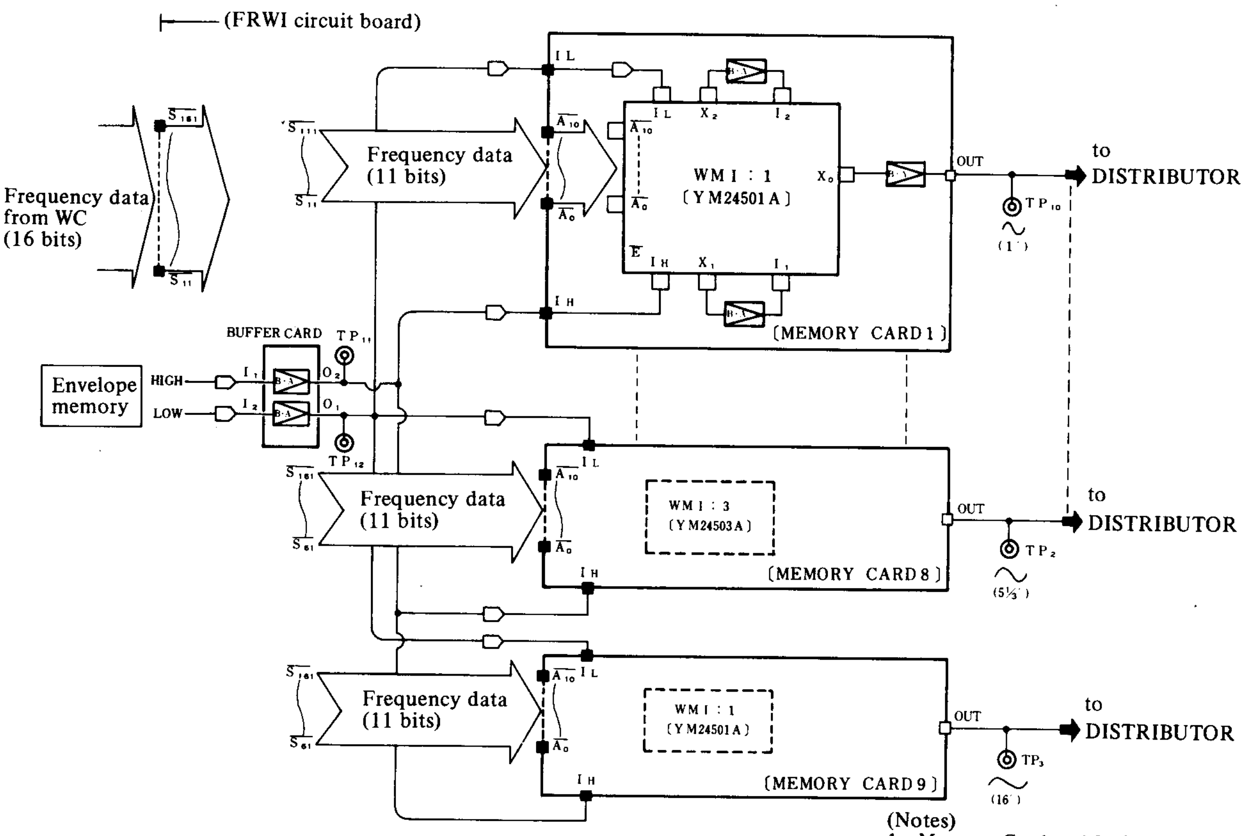
[Fig. 52] PAS Basic Construction Block Diagram

- **Basic Circuit Construction**
  - (1) Sine Wave Memory Circuit
    Memorizes the sine waves for the source of flute tone within respective IC in it's coupler.
  - (2) Distribution Circuit
    Distributes the sine waves to each keyboard.
  - (3) Mixing Circuit
    Synthesizes the sine waves. That is, flute tones are produced that the overtones are added to the fundamental.

4 — 1 ● SINE WAVE MEMORY CIRCUIT

1. Point

- The sine waves for the flute-like tones are memorized within respective IC (Wave Memory) according to the coupler. They are read out by 11-bit frequency data from Wave Counter.
- The same number of sine waves as IC's (Wave Memory) are produced at a time.



(Notes)
1. Memory Cord and Buffer Cord are built in FWM 1 circuit board.
2. This circuit shows the first succession circuit on model E-70.
3. ■ Input terminal on circuit board.

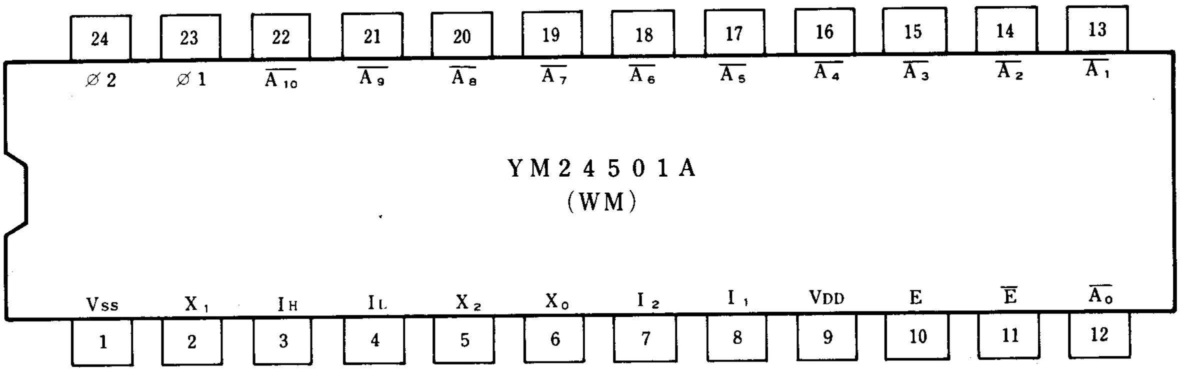
[Fig. 53] Basic Construction of Sine Wave Memory Circuit

2. Basic Circuit Construction

This is made up of a number of IC's (sine wave memory) in the same number as the couplers.
Moreover, the types of Sine Wave Memory IC's are:

- YM24501 (WMI: 1)
  for Fundamentals (1', 2', 4', 8', 16', 32')
- YM24503 (WMI: 3)
  for 5th (1-1/3', 2-2/3', 5-1/3')
- YM240505 (WMI: 5)
  for 3rd (1-3/5', 6-2/5')

3. Explanation of YM24501 (WMI: 1) Terminals

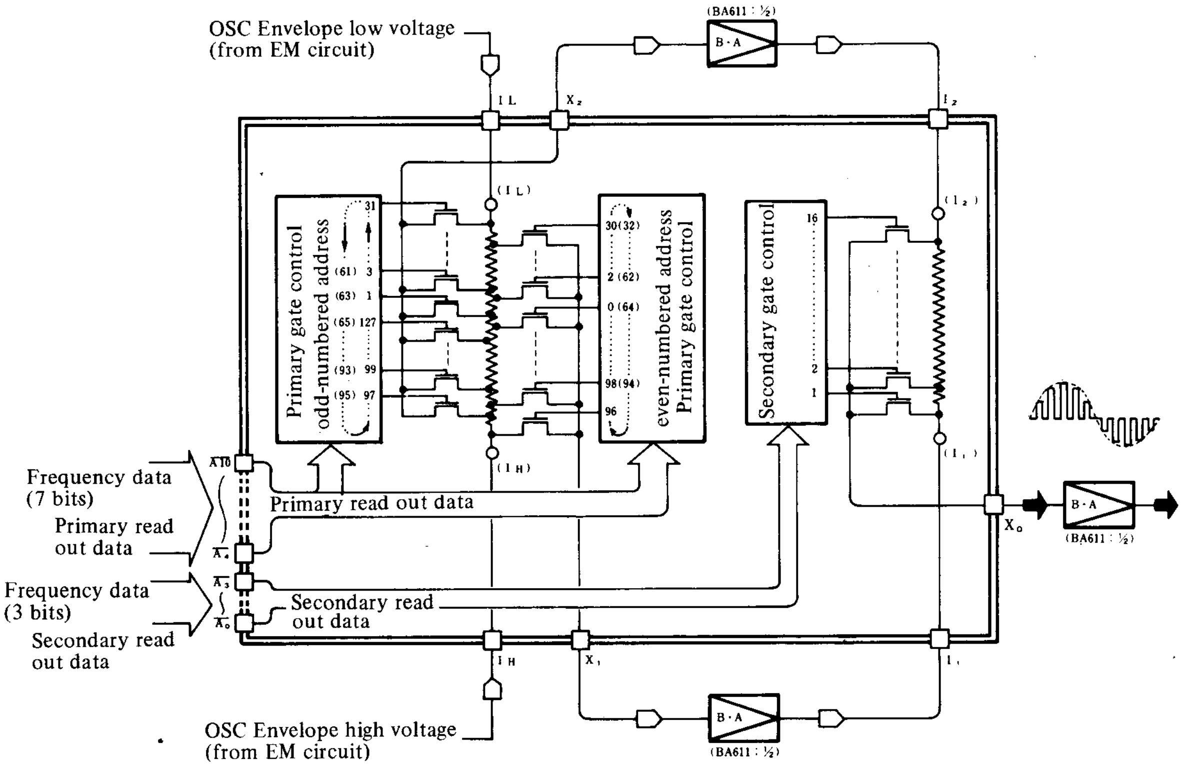


Terminal No.	Code	Designation	Significance	Terminal No.	Code	Designation	Significance
1	Vss	———	Power source (0V)	24	Ø2	Master clock	f ≒ 891 kHz ϕ_1 is opposite phase from ϕ_2
2	X_1	———	Primary output 1 (to AC BUFF)	23	Ø1	〃	
3	I_H	———	Input voltage (HIGH) (−5V Max)	22	$\overline{A_{10}}$	———	Frequency data (Sine wave read out) Input terminal
4	I_L	———	Input voltage (LOW) (0V Max)	21	$\overline{A_9}$	———	
5	X_2	———	Primary output 2 (to AC BUFF)	20	$\overline{A_8}$	———	
6	X_0	———	Sine wave output	19	$\overline{A_7}$	———	
7	I_2	———	Secondary input 2 (to AC BUFF)	18	$\overline{A_6}$	———	
8	I_1	———	Secondary input 1 (〃)	17	$\overline{A_5}$	———	
9	VDD	———	Power source (−15V)	16	$\overline{A_4}$	———	
10	E	ENABLE	IC control by DF	15	$\overline{A_3}$	———	
11	$\overline{E}$	〃	IC control by A_1	14	$\overline{A_2}$	———	
12	$\overline{A_0}$	———	※	13	$\overline{A_1}$	———	※

(Remark) IC's (WM) for 3rd and 5th are same as the above table

[Fig. 54]

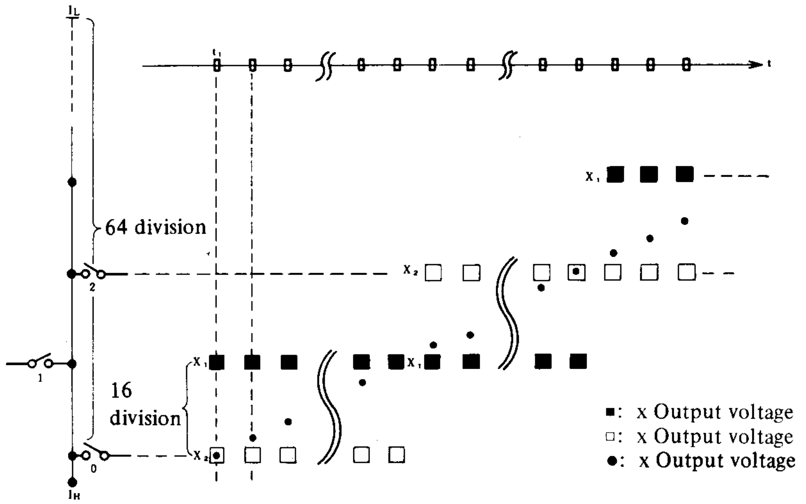
4. Principle of Wave Memory



[Fig. 55] Block Diagram of the WMI IC

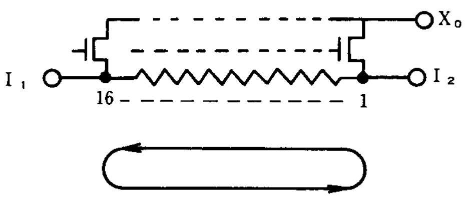
- The IC's of this WM, while dividing the voltage applied to the I_H terminals and the I_L terminals into 64 parts so that the wave patterns will be of the respective sampling oscillation width value at the time of time sharing, are also constructed so that the voltage at each sampling point can be obtained as desired through a switching action.
  This switching action is controlled by the 7-bit code data added to the input terminals $\overline{A_4} \sim \overline{A_{10}}$ of the IC's of the WM, and according to this input data code two successive sampling voltages can be read together. The two sampling voltages read are again input into the I_1, I_2 terminals of the IC of WM through the buffer amp output from each X_1, X_2 terminals at the same time.
  On the other hand, within the IC there is a division of 16 parts between terminal I,and terminal I_2. Each sampling voltage is so constructed that it can be picked out in accordance with the 4-bit code data input from the IC input terminals $\overline{A_0} \sim \overline{A_3}$, and the sampling voltage picked out is output to X_0.
  The WM carries out two actions at the same time. Therefore, with the input data of $\overline{A_4} \sim \overline{A_{10}}$, the voltage X and X_2 adjoining the sampling voltage between the terminals I_H and I_L are taken out, and moreover during this period output is made at X_0 after fine sampling with the input data of $\overline{A_0} \sim \overline{A_3}$.

(Example) **[Fig. 56]**

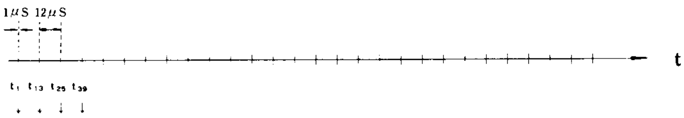


(Note 1) The adjacent gates, odd-numbered gate and even-numbered gate, are turned on at a time to fed out the output voltages X_1 and X_2.

(Note 2) The order of the gate movement by 4-bit data $\overline{A_0} \sim \overline{A_3}$. **[Fig. 57]**

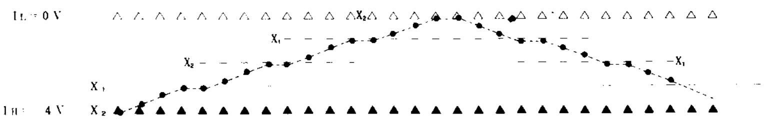


(Example) Assuming that WM activates with 5-bit input frequency data when I_H is –4V and I_L is 0V.



Gate control 2 control data $\overline{A_1}(2^0)$	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Gate control 2 control data $\overline{A_2}(2^1)$	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
Gate control 1 control data $\overline{A_3}(2_2)$	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
Gate control 1 control data $\overline{A_4}(2_3)$	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gate control 1 control data $\overline{A_5}(2^4)$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Decimal notation	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	------														
X_1 (V)	-3	-3	-3	-3	-3	-3	-3	-3	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	---							
X_2 (V)	-4	-4	-4	-4	-2	-2	-2	-2	-2	-2	-2	-2	0	0	0	0	0	0	0	0	-2	-2	-2	-2	---							
X_0 (V)	-4	-3.7	-3.3	-3	-3	-2.7	-2.3	-2	-2	-1.7	-1.3	-1	-1	-0.7	-0.3	0	0	-0.3	-0.7	-1	-1	-1.3	-1.7	-2	---							

(Note) "0" ≒ 0V
"1" ≒ –15V



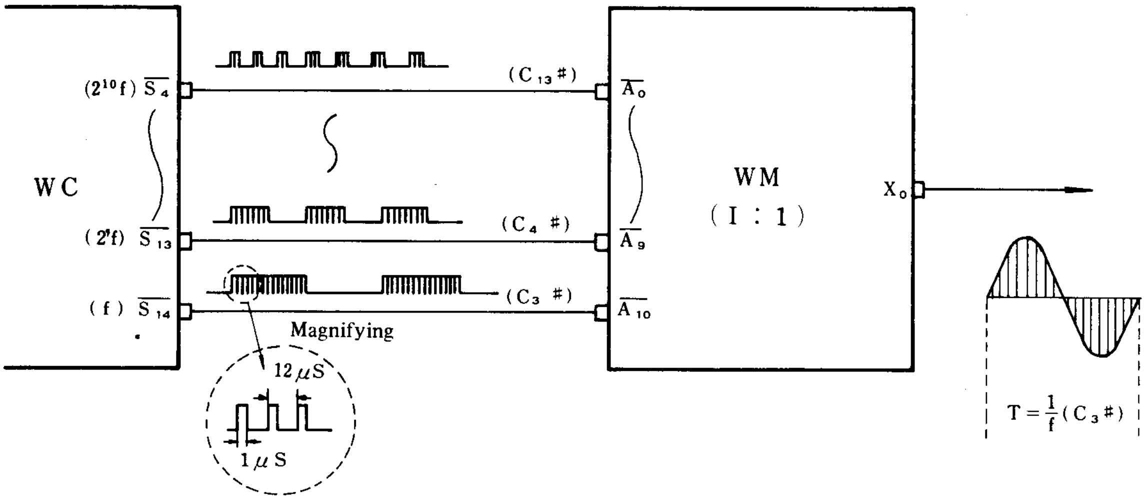
(Note) △ = IL Voltage
▲ = IH Voltage
– = X_1 and X_2 Voltage
● = X_0 Output voltage

5. Outline of the WM Movement

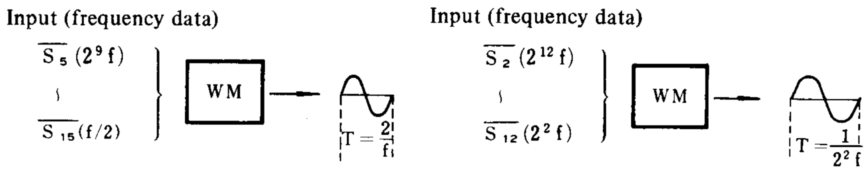
Fine sampling for numerous voltages based on the voltages between the I_L and I_H terminals are provided to produce sine waves. The 11 bit code data input from WC is used to produce a sine wave with a single interval while reading the sampling voltage through time sharing.

That is, of the 16 bit frequency data prepared through time sharing with the WC the 11 bit frequency data is input into WM and in accordance with this input code data phasing of the wave pattern is carried out by reading the desired sampling voltage. This reading period is determined by the longest frequency period of the 11 bit frequency data.

(Example) Assuming that Key $C_3^{\#}$ is pressed when the $S_4 \sim S_{14}$ (11 bits) terminals of WC are connected to the corresponding input terminals $A_0 \sim A_{10}$ (11 bits) of WM. [Fig. 58]



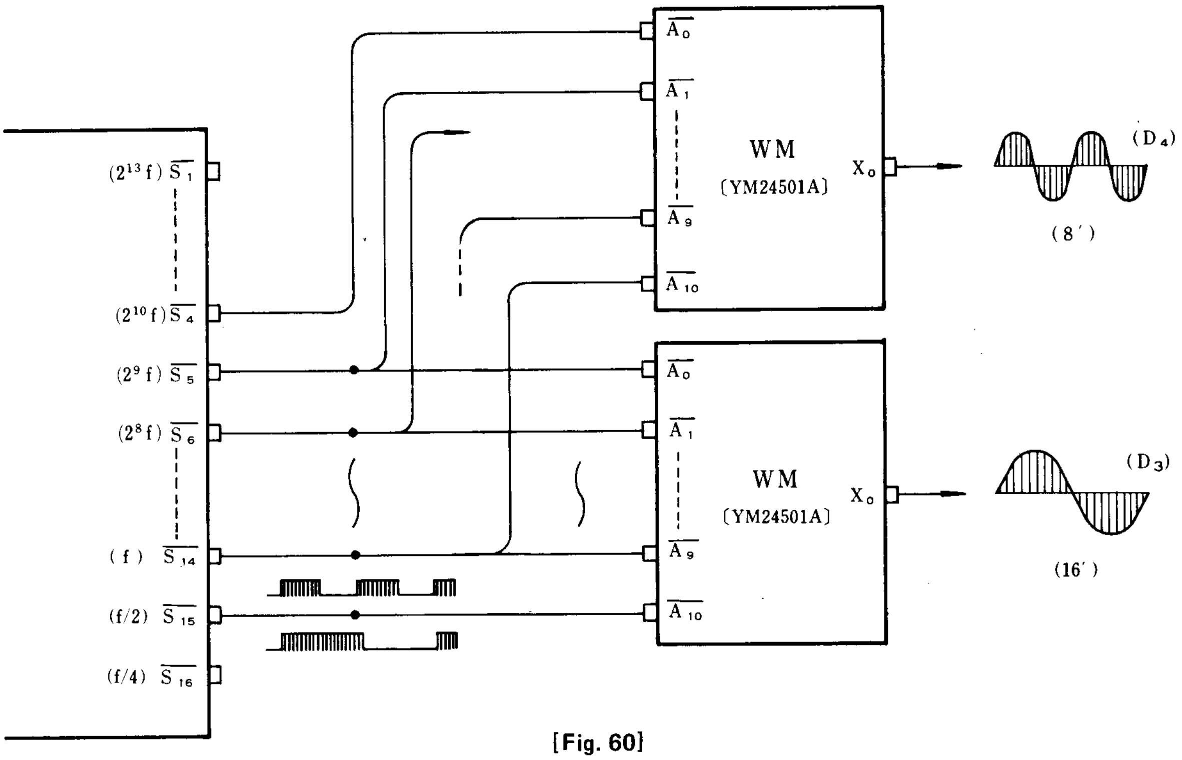
(Example) When the key of frequency f is depressed. **[Fig. 59]**



(Note) The above shows the IC of fundamental WM.

- In this way, with the 11 bit frequency data corresponding to one key (i.e., one channel), the WM reads out each sampling voltage every 12μS interval for preparing the sine wave with the interval matched to the key. Therefore, by providing a number of WM's having similar functions, and by changing (shifting one terminal at a time) the method of wiring connection, the 11 bit data from the WC will be changed and the WM's will generate coupler sounds simultaneously to one key.

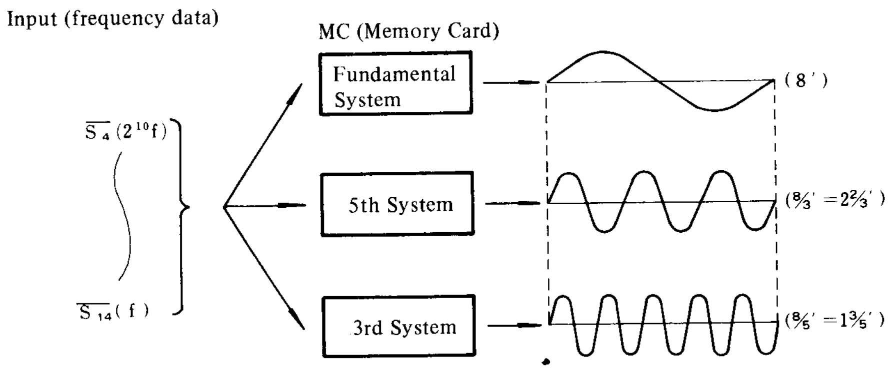
(Example) When two WM's are provided and the wiring connected as follows (press key D_4).



[Fig. 60]

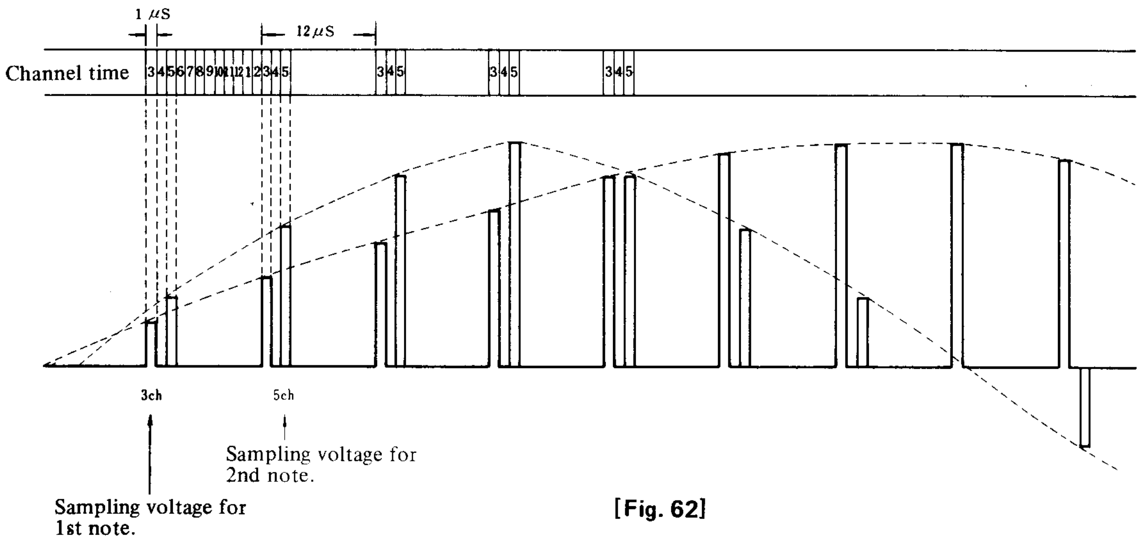
- Moreover, according to the code 11 bit input frequency data, the ICs of 3rd-System (YM24505A) and 5th-System (YM24503A) proceed the gate address steps with the speed 5 times and 3 times faster than that of fundamental System IC (YM24501A).
  That is, when the same frequency is fed into these ICs, 3rd-System IC output 5 cycles of wave while 5th-System IC 3 Cycles, during the time the fundamental System IC output one cycle.

(Example) **[Fig. 61]**



The 2-2/3' tones are obtainable in connecting the WC terminals $\overline{S_4} \sim \overline{S_{14}}$ to the 5th-System IC. In the same manner, 3rd-System tones are obtainable as well as other 5th-System tones.

As the reading of this sampling voltage is carried out for each channel, the output of the sine wave for the maximum of 12 sounds is shifted in time from the output terminal X_0 of the WM IC's.



[Fig. 62]

7. $\overline{E}$ (Enable) Terminal

The WM Functions only when the $\overline{E}$ terminal is placed to "0" (≒ 0V)

The $\overline{A1}$ data (Channel occupation data) produced in CLP is fed into this WM $\overline{E}$ terminal so that the WM operates in accordance with the key pressed.

6. Envelope Voltage (I_H, I_L Terminal Voltage)

To the terminals I_H and I_L, time shared voltage (envelope voltage) for each channel sent from the Envelope Control Circuit (explained later) is added.

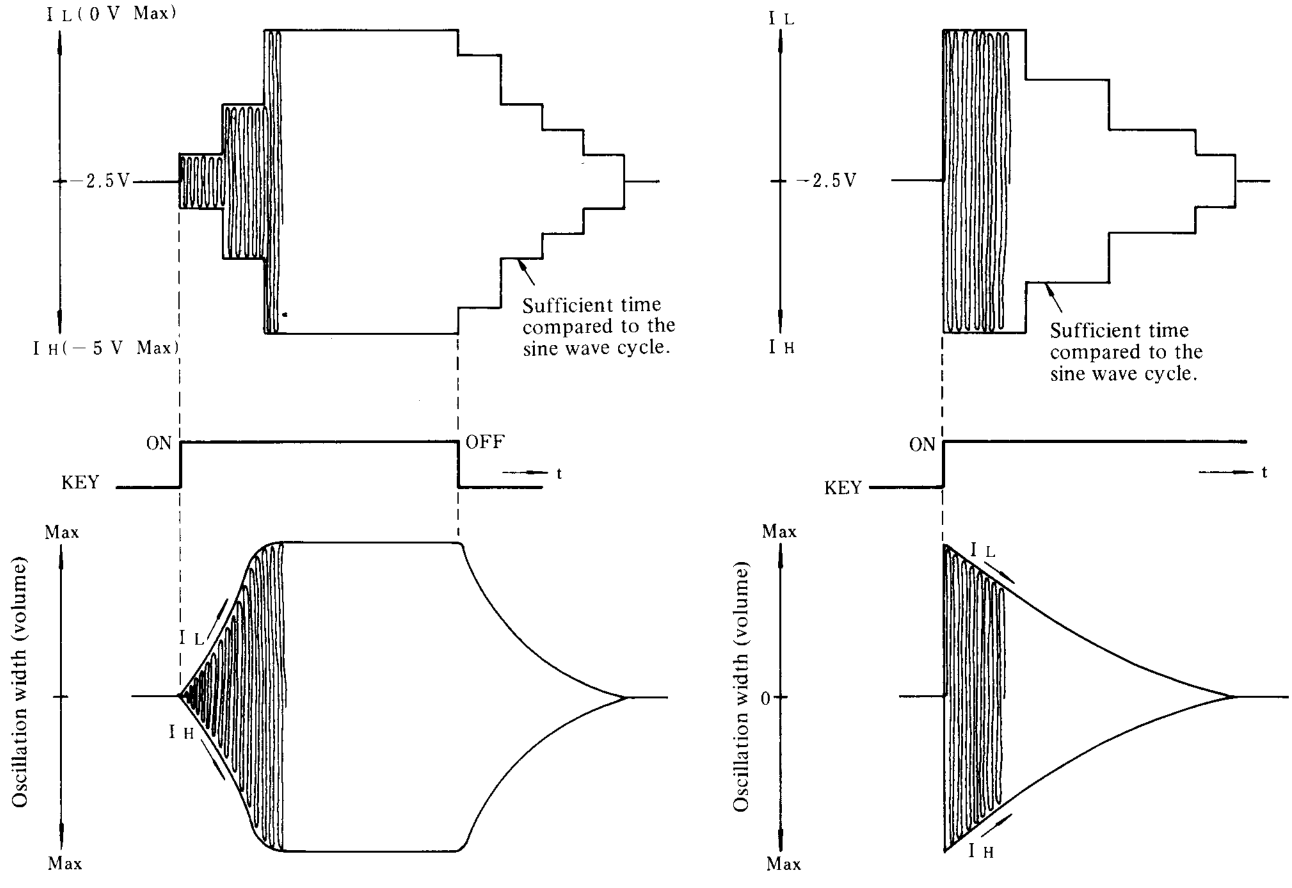
The WM creates the sampling voltage for shaping a sine wave by dividing the voltage given between the terminals I_H and I_L. (In other words, the voltage between I_H and I_L means the maximum amplitude of the sine wave produced.)

Therefore, if the voltage added to the terminals I_H and I_L are varied in sufficiently long time as compared with one cycle of the sine wave produced by WM, the maximum amplitude of the sine wave can be changed.

That accounts for how the envelope of the flute family tones are controlled.

(Example) Voltage change between terminals I_H and I_L at Sustain mode.

(Example) Voltage change between terminals I_H and I_L at Attack mode.



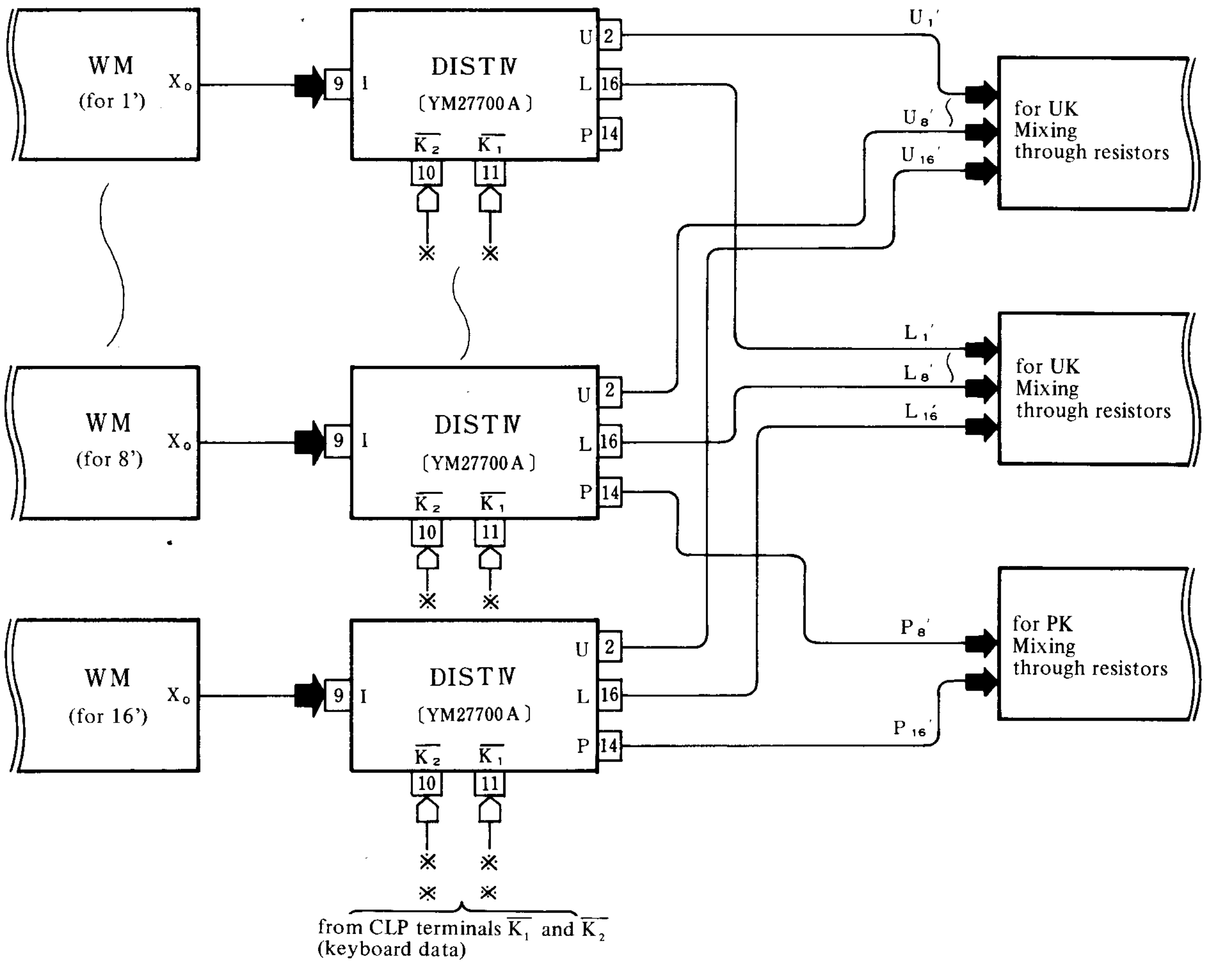
[Fig. 63]

The voltage between I_H and I_L is raised to 5V (I_H = −5V, I_L = 0V) at one time and the phase difference decreased gradually. (ATTACK mode)

4 — 2 ● DISTRIBUTOR

1. Point

- The Distributor is a circuit which uses the keyboard data ($\overline{K_1}$, $\overline{K_2}$) from the CLP to distribute, by keyboard, the numerous sine waves made in the sine wave generating circuit.
- Since at each Wave Memory of the sine wave generation circuit a single interval sound common to the UK, LK, and PK is created, this Distributor serves to distribute them by keyboard and adds the sound source waves of each keyboard to the Mixing Circuit for each.



[Fig. 64] Basic Construction of the Distributor

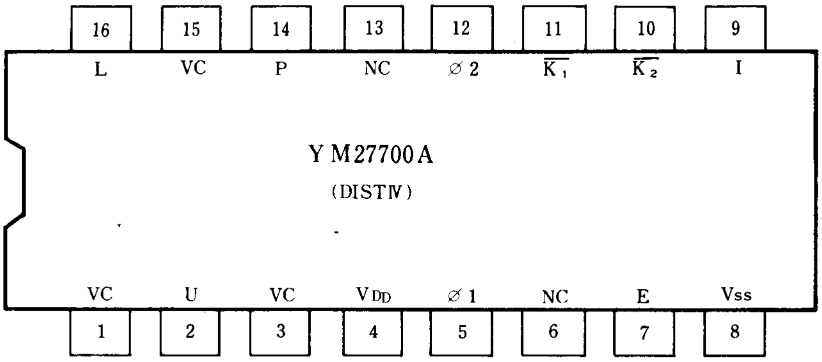
2. Basic Construction of the Circuit

Consisting of:

- For flute tones: DISTRIBUTOR IV (YM27700A: DIST IV).
- For attack tones: DISTRIBUTOR V (YM28000A: DIST V)

(Note) DIST IV receives 2 input while DIST V 1 input.

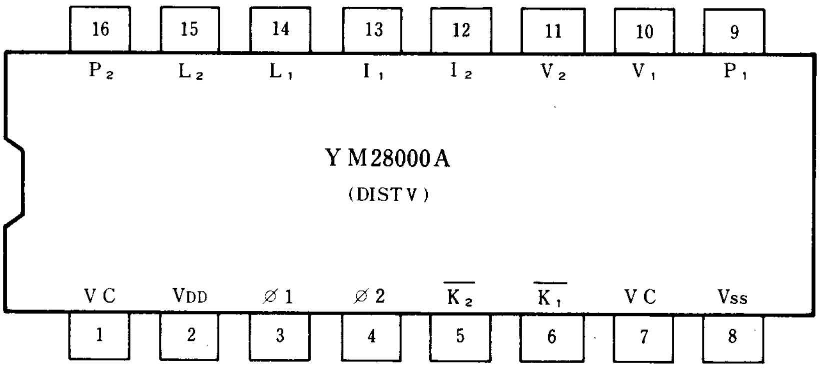
3. Explanation of YM27700A (DIST IV) Terminals



Terminal No.	Terminal Code	Designation	Significance	Terminal No.	Terminal Code	Designation	Significance
1	VC	−2.5V	Center (bias) voltage	16	L	————	LK channel output
2	U	————	UK channel output	15	VC	————	
3	VC	————		14	P	————	PK channel output
4	VDD	————	Power source (−15V)	13	NC	————	
5	Ø1	————	Master clock (f ≒ 891 kHz)	12	Ø2	ϕ_2 is opposite phase from ϕ_1	Master clock
6	NC	————		11	$\overline{K_1}$	————	Keyboard data input (from CLP)
7	E	ENABLE	IC functions at "1" (−15V) (fixed)	10	$\overline{K_2}$	————	
8	Vss	————	Power source (0V)	9	I	————	Tone source wave form input (from WM)

[Fig. 65]

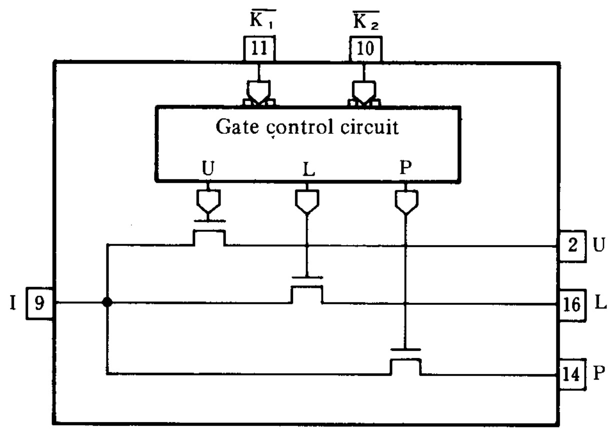
(Reference) Explanation of YM27700A (DISTV) Terminals



[Fig. 66]

4. Actions of the Distributor

The Distributor a gate circuit for UK, LK, and PK, and is controlled by the keyboard data ($\overline{K_1}, \overline{K_2}$: 2 bits)



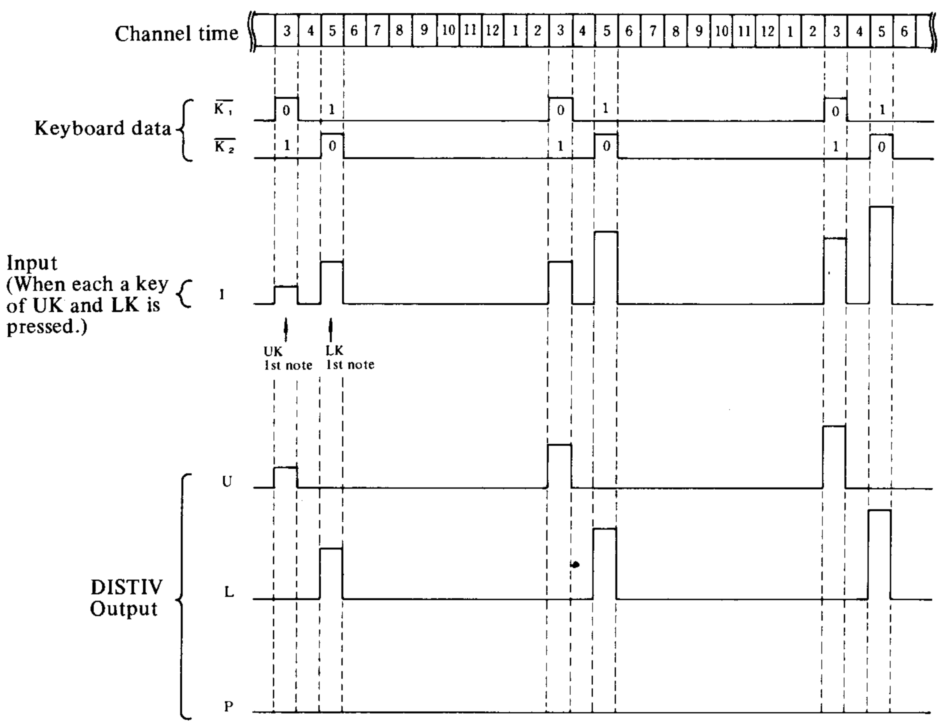
[Fig. 67] Block Diagram of DISTIV IC

A sampling voltage which forms the sine waves for each respective channel time is fed into the DIST IV terminal I of each of the 12 channels by time sharing from one of the WM circuits.

Also, the keyboard data ($\overline{K_1}, \overline{K_2}$), which indicates to which channel each keyboard sound is allocated, is also added through time sharing with absolutely the same timing as the input of the Distributor from CLP.

Therefore, the sine wave of each channel input into Terminal I is distributed, by keyboard, by $\overline{K_1}, \overline{K_2}$.

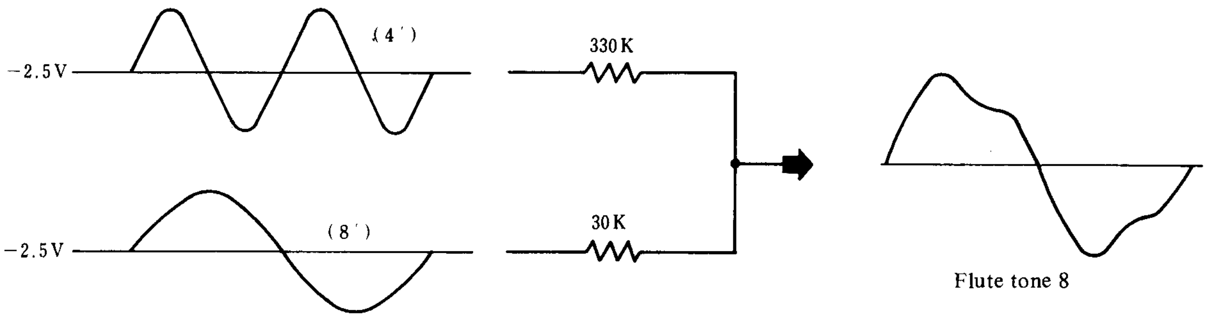
(Example)



[Fig. 68]

4 — 3 ● MIXING CIRCUIT

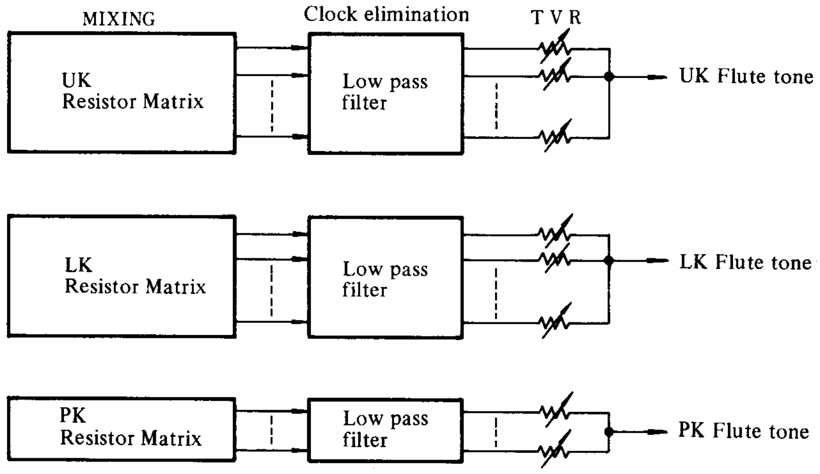
The flute-like tone contains a small amount of low overtones to the basic waves. Therefore each oscillation width level of the numerous sine waves read out from the sine wave memorizing circuit is of the same level; this circuit adjusts the oscillation width of each following overtone, and by mixing makes a more natural flute-like tone.



[Fig. 69]

This Mixing Circuit is composed of a resistor matrix, there is a circuit for each keyboard.

(Reference) Basic Block Diagram from Mixing Circuit to Tone Lever [Fig. 70]

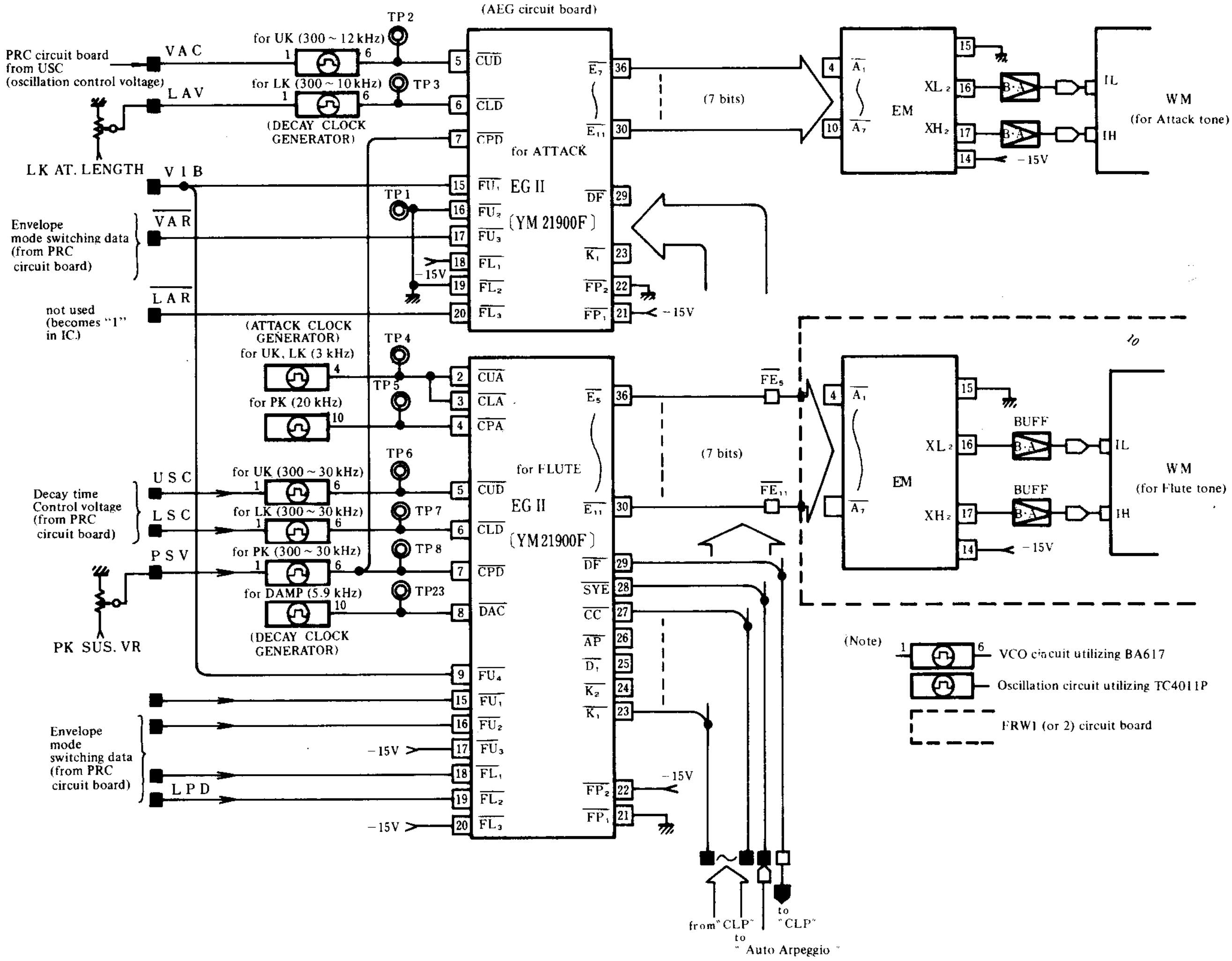


Between the mixing circuit and the tone lever there is a Low Pass Filter Circuit to eliminate clockpulses.

4 — 4 ● ENVELOPE CONTROL CIRCUIT (FLUTE TONES)

1. Point

- This Envelope Control Circuit controls the time shift of the sound volume level from the start of the flute sound to its decay.
- Two kinds of circuits, for Attack Tone and for Flute Tone, are built in the circuit according to the difference of envelope mode.
- This functions in absolutely the same timing as the movement of ROM → WC → WM.



(Basic Construction of Flute Tones Envelope Control Circuit on E-70) **[Fig. 71]**

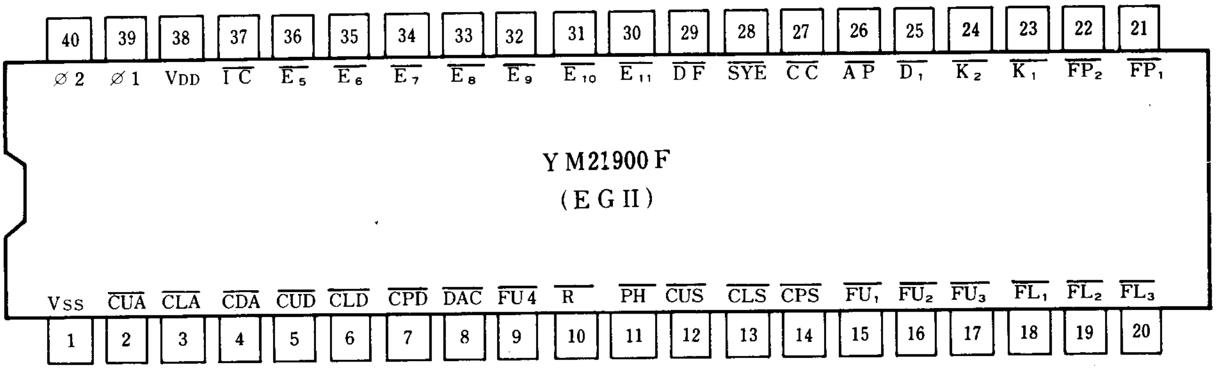
2. Basic Circuit Construction

The basic circuit construction is made up of the following two IC's:

- Envelope Generator II (EG II):
  Control the time to read out the envelope voltage memorized in EM.
- Envelope Memory (EM):
  Memorizes the envelope voltage and output it to WM according to the data from EG II.

In addition to the above there are clock generator IC's such as Attack Clock and Decay Clock which determine the time to read out the envelope voltage.

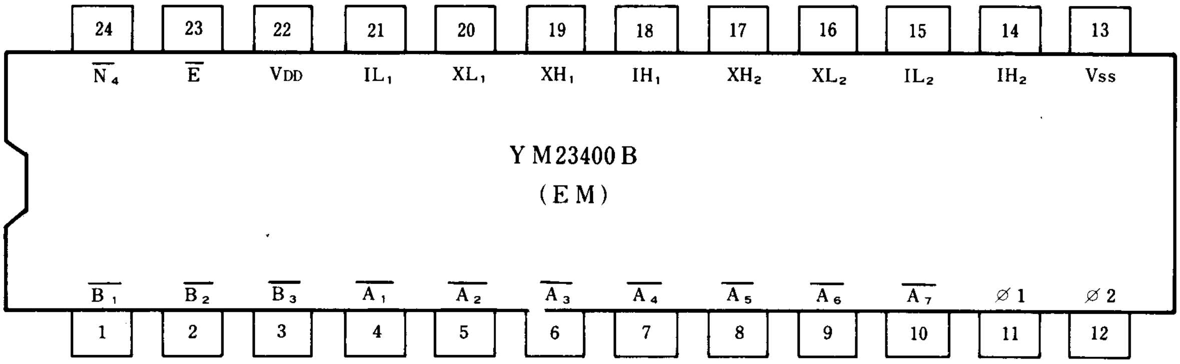
3. Explanation of YM21900F (EGII) Terminals



Terminal №.	Terminal Code	Designation	Significance	Terminal №.	Terminal Code	Designation	Significance
1	Vss	——	Power source (0V)	40	Ø2	Master clock	(f = 891 kHz) ϕ_1 is opposite phase from ϕ_2
2	$\overline{CUA}$	CLOCK UPPER ATTACK	Clock pulse input for UK Attack	39	Ø1		
3	$\overline{CLA}$	CLOCK LOWER ATTACK	Clock pulse input for LK Attack	38	VDD	——	Power source (−15V)
4	$\overline{CPA}$	CLOCK PEDAL ATTACK	Clock pulse input for PK Attack	37	$\overline{IC}$	——	Input; Clears all counters and S/R when switch is ON.
5	$\overline{CUD}$	CLOCK UPPER DECAY	Clock pulse input for UK Decay	36	$\overline{E_5}$	——	EG Counter output (7 bits to EM)
6	$\overline{CLD}$	CLOCK LOWER DECAY	Clock pulse input for LK Decay	35	$\overline{E_6}$	——	〃
7	$\overline{CPD}$	CLOCK PEDAL DECAY	Clock pulse input for PK Decay	34	$\overline{E_7}$	——	〃
8	$\overline{DAC}$	DAMP CLOCK	Clock pulse input for Damper	33	$\overline{E_8}$	——	〃
9	$\overline{FU_4}$	FUNCTION UPPER 4	UK Envelope Mode Switching Function input terminal ("0" when vibraphon ON)	32	$\overline{E_9}$	——	〃
10	$\overline{R}$	——	NC	31	$\overline{E_{10}}$	——	〃
11	$\overline{PH}$	——	NC	30	$\overline{E_{11}}$	——	〃
12	$\overline{CUS}$	CURVE UPPER SELECT	UK Envelope curve selection	29	$\overline{DF}$	DECAY FINISH	Decay finish data output
13	$\overline{CLS}$	CURVE LOWER SELECT	LK 〃	28	$\overline{SYE}$	SYNCHRO ENABLE	used for Auto Arpeggio
14	$\overline{CPS}$	CURVE PEDAL SELECT	PK 〃	27	$\overline{CC}$	COUNTER CLEAR	Input data to clear the counter by KEY-ON, KEY-ON AGAIN, KEY-OFF etc. (from CLP)
15	$\overline{FU_1}$	FUNCTION UPPER 1	UK Envelope mode switching Function input terminal	26	$\overline{AP}$	ATTACK PULSE	One pulse sent out when keyboard is on. (from CLP)
16	$\overline{FU_2}$	〃 〃 2		25	$\overline{D_1}$	DECAY	Becomes command to start when decay starts, with keyboard OFF signal. (from CLP)
17	$\overline{FU_3}$	〃 〃 3		24	$\overline{K_2}$	KEYBOARD DATA 1	Keyboard data input (from CLP)
18	$\overline{FL_1}$	〃 LOWER 1	LK Envelope mode switching Function input terminal	23	$\overline{K_1}$	〃 2	
19	$\overline{FL_2}$	〃 〃 2		22	$\overline{FP_1}$	FUNCTION PEDAL 2	PK Envelope mode switching Function input terminal
20	$\overline{FL_3}$	〃 〃 3		21	$\overline{FP_2}$	FUNCTION PEDAL 1	

[Fig. 72]

4. Explanation of YM23400B (EM)

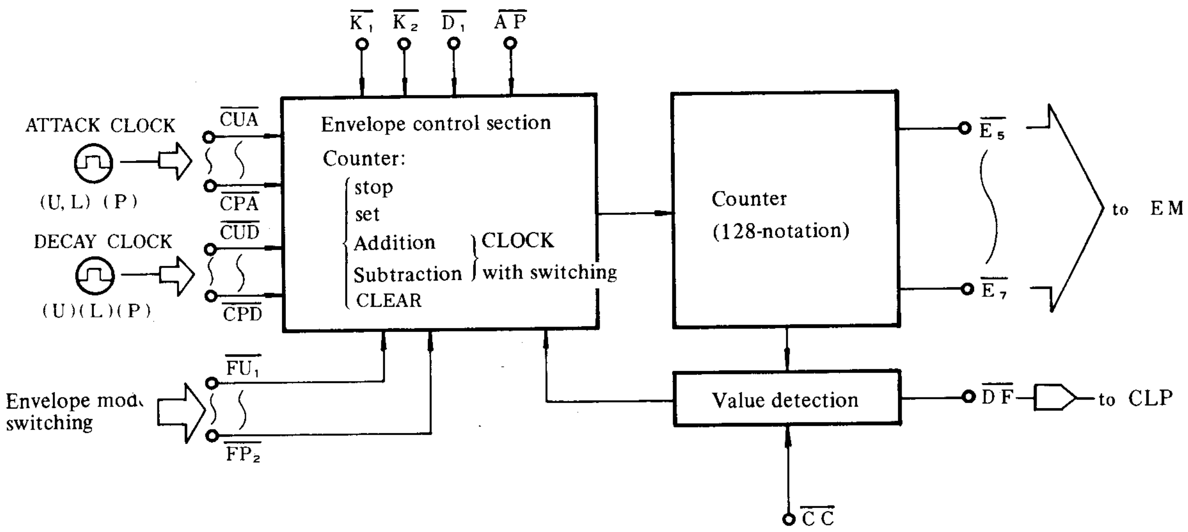


Terminal №.	Terminal Code	Designation	Significance	Terminal №.	Terminal Code	Designation	Significance
1	$\overline{B_1}$	BLOCK DATA	Block data input (not used)	24	$\overline{N_4}$	NOTE DATA	not used
2	$\overline{B_2}$	〃		23	$\overline{E}$	ENABLE	IC functions at "0" (from $\overline{A_1}$ of CLP)
3	$\overline{B_3}$	〃		22	VDD	———	Power source (−15V)
4	$\overline{A_1}$	———	Gate address data input terminal (Input the count output value of EGII)	21	IL_1	———	not used
5	$\overline{A_2}$	———		20	XL_1	———	
6	$\overline{A_3}$	———		19	XH_1	———	
7	$\overline{A_4}$	———		18	IH_1	———	
8	$\overline{A_5}$	———		17	XH_2	———	Envelope voltage wave shape output
9	$\overline{A_6}$	———		16	XL_2	———	
10	$\overline{A_7}$	———		15	IL_2	0 V	DC voltage for envelope
11	Ø1	Master clock	ϕ_2 is opposite phase from ϕ_1.	14	IH_2	− 5 V	
12	Ø2	〃	(f ≒891kHz)	13	Vss	———	Power source (0V)

[Fig. 73]

5. Principle of EM II Movement

- Of the keyboard data generated by the CLP, the EGII uses data $\overline{K_1}$, $\overline{K_2}$, $\overline{AP}$, and $\overline{D_1}$ to include the Attack Clock Pulse and the Decay Clock Pulse. The pulses which have been taken in are calculated with the Counter, and the calculated figures are fed out as 7 bit ($\overline{E_5} \sim \overline{E_{11}}$) codes. This output data becomes the address code data for reading the sampling voltage, which samples the envelope waves memorized in the EM circuit (explained later).



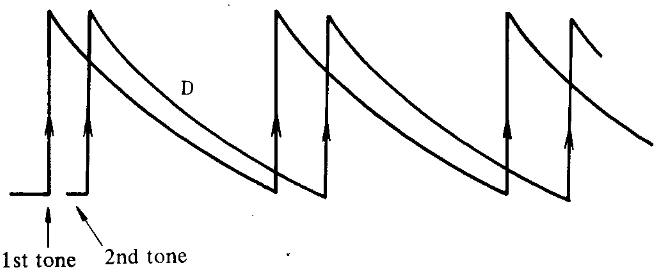
[Fig. 74] (Block Diagram of EGII IC)

- First, with the keyboard data ($\overline{K_1}$, $\overline{K_2}$), that indicates to which keyboard, UK, LK, or PK the key pressed belongs, among the keyboard data from the CLP, it can be known which keyboard key is allocated to which channel of the 12 channels.

- Next, the voltage mode added to the terminals $\overline{FU_1} \sim \overline{FU_3}$, and $\overline{FP_1} \sim \overline{FP_2}$ determines, according to the function selector switch (for each channel, each keyboard), what kind of envelope wave to generate to the key data allocated to each channel.

- Moreover, the Attack Clock Generator to determine the tone rising time (Attack Time) and the Decay Clock Generator to determine the tone decaying time (Decay Time) are prepared for each keyboard.
  With keyboard data ($\overline{K_1}$, $\overline{K_2}$), EGII discriminates which keyboard tone is allocated to which channel and at the same time, it takes into clock pulse for each keyboard by channels.
  The pulse taken into is computed by the counter for each channel and then, the envelope voltage is read out in order according to the computed value from EM (explained later).
  Since the Attack Time and Decay Time allocated to each channel are controlled by each keyboard and the notes are processed by pulse count by time sharing in accordance with each channel, each tone can be independently controlled with Attack and Decay.

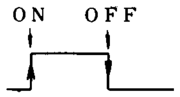
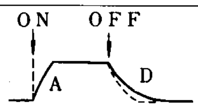
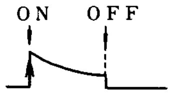
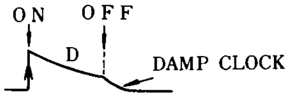
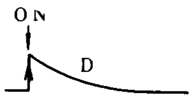
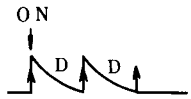
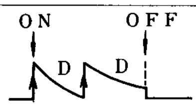
(Example) In the case of Attack Repeat Effect ($\overline{FU_1} = 1, \overline{FU_2} = 0, \overline{FU_3} = 0$)



[Fig. 75]

- D (= Decay Time)
- The frequency of UK decay clock pulse is controlled by Attack Length lever, while $\overline{FU_1} \sim \overline{FU_3}$ mode, by Attack Repeat lever.
- Due to the function control data is "$\overline{FU_1} = 1, \overline{FU_2} = 0$ and $\overline{FU_3} = 0$", the attack becomes quick rising regardless of attack clock.

- (EGII Function mode and EM output wave mode)

	E G II				E M	
UK→ / LK→ / PK→	$\overline{FU_1}$ ($\overline{FL_1}$) ($\overline{FP_1}$)	$\overline{FU_2}$ ($\overline{FL_2}$) (FP_2)	$\overline{FU_3}$ ($\overline{FL_3}$) —	Envelope mode	Envelope voltage (EM output wave pattern)	Rise drive data
	1	1	1	Direct keying mode	 ON OFF	$\overline{AP}$
	0	1	1	Sustain mode	 ON OFF A D	$\overline{K_1}$、$\overline{K_2}$
	1	0	1	Purcussive damp mode ($\overline{FU_4} = 1$)	 ON OFF	$\overline{AP}$
	1	0	1	Purcussive damp mode ($\overline{FU_4} = 0$)	 ON OFF D DAMP CLOCK	$\overline{AP}$
	0	0	1	Purcussive mode	 ON D	$\overline{AP}$
	1	0	0	Purcussive repeat damp mode	 ON D D	$\overline{AP}$
	0	0	0	Purcussive repeat damp mode	 ON OFF D D	$\overline{AP}$

[Fig. 76]

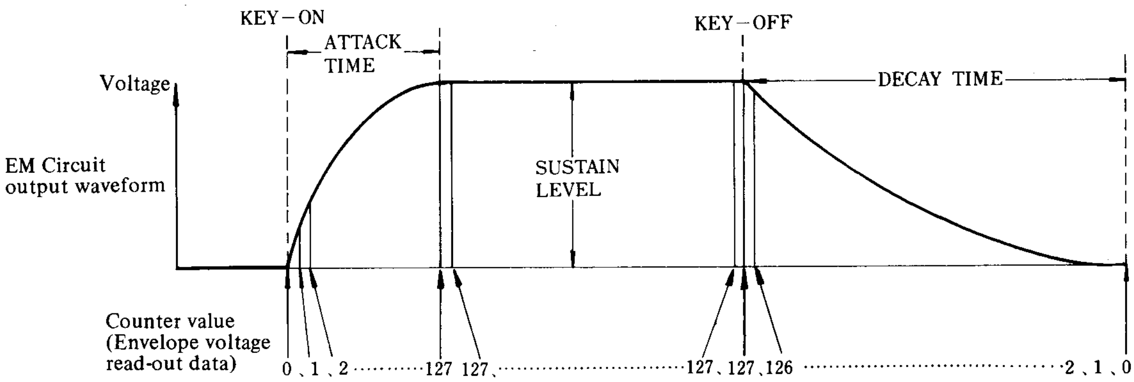
(Note) $0 \fallingdotseq 0V$
$1 \fallingdotseq -15V$

Notes:
1. The ↑ and ↓ become quick rises and falls regardless of external clock.
2. $\overline{FU_3}$ ($\overline{FL_3}$) of flute tone EGII is fixed to "1" and $\overline{FU_2}$ ($\overline{FL_2}$) of attack tone EGII to "0". $\overline{FU_3}$ ($\overline{FL_3}$) is controlled by Attack Repeat lever.
3. $\overline{FU_4}$ is provided for only flute tone EGII and can be turned to "0" only when vibraphone lever is ON.
4. The PK mode is controlled by the 2-bit code of FP_1 and FP_2. (FP_3 is fixed to "1" within the IC)
   Still more, on E-70 it is fixed as:
   Flute tone: Sustain mode
   Attack tone: Purcussive damp mode

6. EG II Movement on Each Mode

(1) During Sustain Mode

- At the same time the key is pressed, the data $\overline{K_1}, \overline{K_2}$ (generating in the CLP) is added to the counter in the IC after being received by the attack clock by channel.
- The counter calculates these clock pulses, counting from 0 to 127, and when 127 is reached attack clock pulse reception is stopped by a control in the IC.
- The calculation conditions from 0 to 127 are changed to a 7-bit code to become read out data (address data) of each sampling voltage, memorized by the EM and to terminals $\overline{E_5} \sim \overline{E_{12}}$. (ATTACK TIME)
- Moreover, this EG II repeats the calculation conditions of the counter at intervals of 1μS pulse width and 12μS per channel, and feeds the 7-bit code data to terminals $\overline{E_5} \sim \overline{E_{12}}$. Therefore, while repeating the address data several times it naturally advances gradually to the 127th step.
- During KEY ON the counter calculations stop as is. Thus, in this condition the 7 bit code data, indicating 127 as the address data, is continuously fed out in order as channel data for the key pressed. (SUSTAIN LEVEL)
- With KEY OFF the decay clock pulse having the clock frequency set by the control lever is received with the decay command data $\overline{D_1}$ sent in from the CLP, and while it is being added to the counter it changes the calculations to the subtraction. Therefore, according to the speed of the clock, the counter counts from 127 to 0. (DECAY TIME)

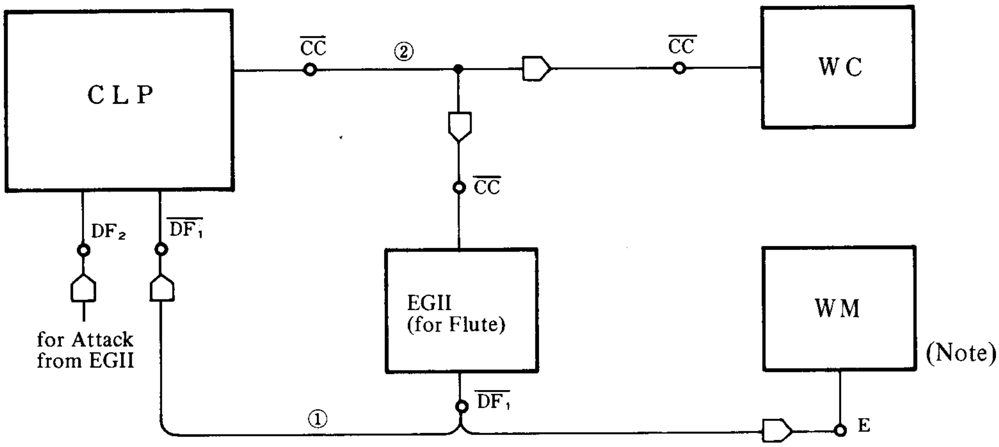


[Fig. 77]

This calculation condition is also fed out as address data to each channel, and so with the frequency of this decay clock the decay time is controlled.

(Example) The frequency of attack clock pulse of the flute tone is fixed.
The frequency of decay clock pulse of the same is controlled by sustain lever.
And also, the sustain mode is determined by the sustain tablet ON.

- Also, when the counter counts to 0, a pulse is fed out to the $\overline{DF}$ terminal and is added to the $\overline{DF}$ terminal of the CLP as decay end data. (The value detector on EG II is continuously detecting the counting conditions of the counter for each channel.)
  Moreover, with this $\overline{DF}$ data the CLP feeds out counter clear $\overline{CC}$ data, and so the channel counter is cleared and returns to the start condition.

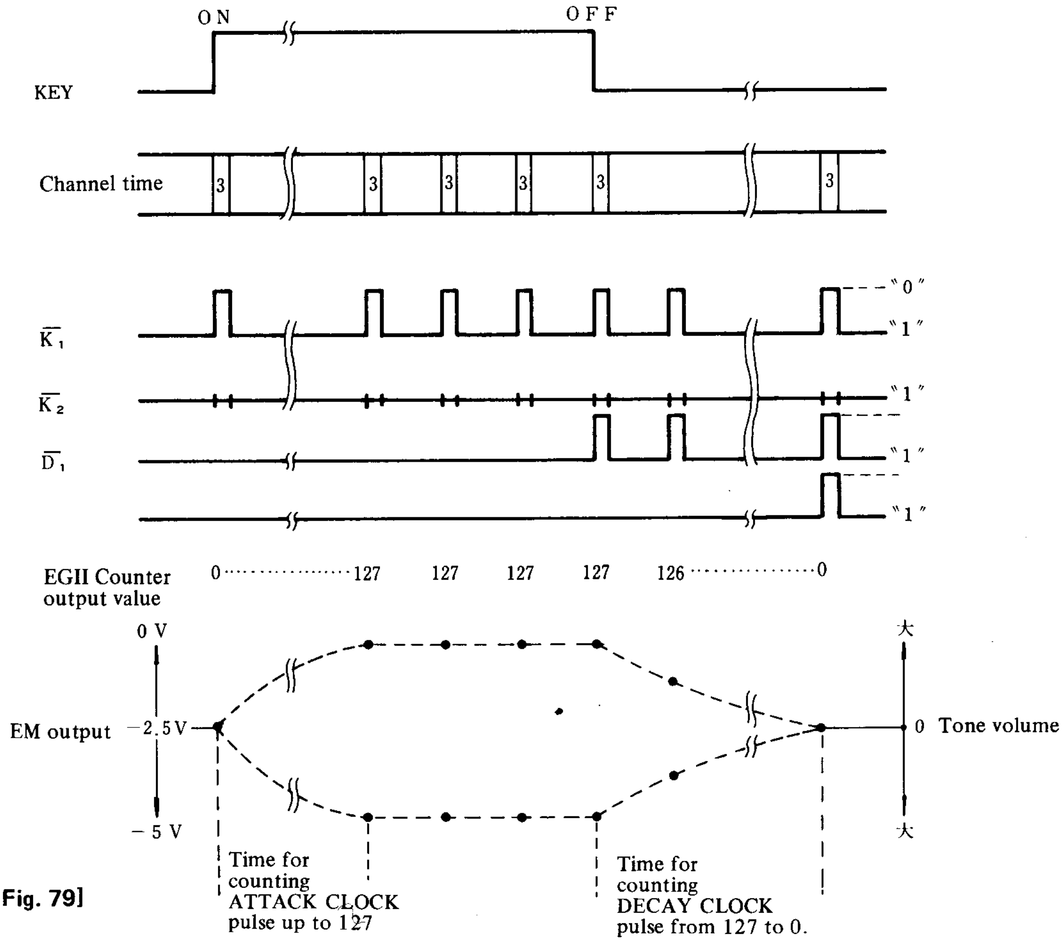


[Fig. 78]

(Note) The WM movement is cancelled by "0" of the E terminal.

- These EG II movement is processed by channels through 12-tone time sharing.

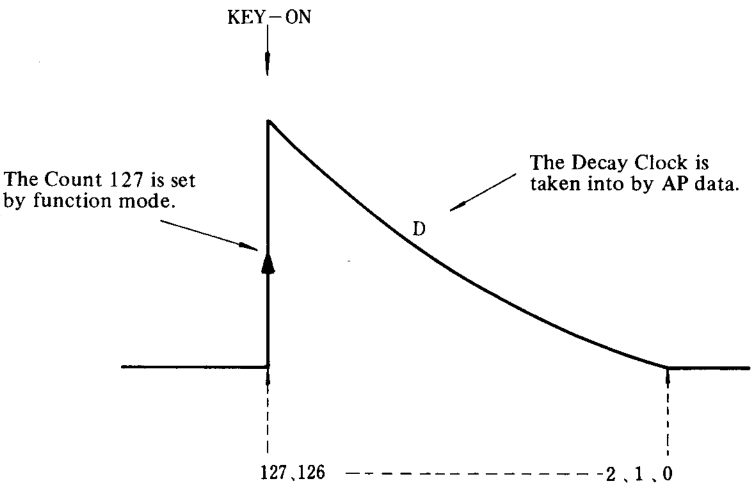
(Reference) The relation between each data and EM output wave during Sustain mode when one UK key is pressed.



[Fig. 79]

(2) EG II Movement During Percussive Mode

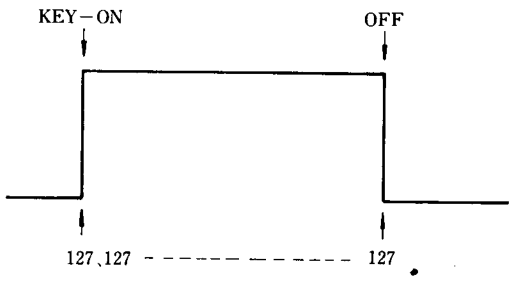
The attack pulse data $\overline{AP}$ is sent out one time (1μS) from the CLP with KEY ON (This pulse synchronizes with the channel the key note is allocated.) When the function switching terminals $\overline{FU_1} \sim \overline{FU_3}$, $\overline{FL_1} \sim \overline{FL_3}$, $\overline{FP_1} \cdot \overline{FP_2}$ are set to the mode condition "0", "0", "1".
With this attack pulse data $\overline{AP}$, the EG II Envelope Control set the counter to the volue 127 suddenly and at the same time it takes into the decay clock pulse.
As the Decay Clock Generators are provided for each keyboard, the decay clock pulse corresponding to each channel and keyboard is received, being descriminated by keyboard data ($\overline{K_1}$, $\overline{K_2}$), according to respective channel time.
With this decay clock pulse, the counter begins subtractive counting from 127 until 0.
This counting is carried on regardless of the key is depressed or not during the above movement.



[Fig. 80]

(3) EG II Movement During Direct Keying Mode

With $\overline{AP}$ data, the EG II Counter is set to "127" regardless of external continuesly output the value 127 during the key is pressed when the function switch terminals ($\overline{FU_1} \sim \overline{FU_3}$, $\overline{FL_1} \sim \overline{FL_3}$, $\overline{FP_1} \sim \overline{FP_2}$) are set to respectively "1", "1", "1".

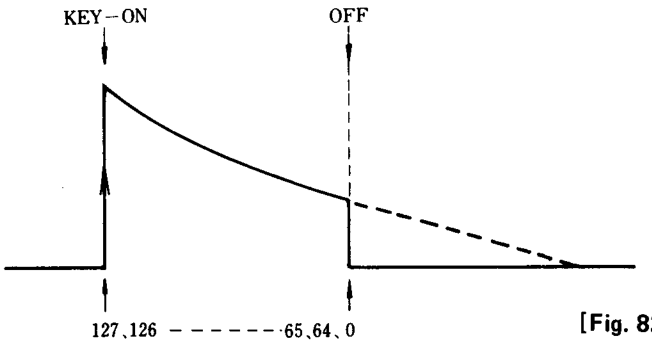


[Fig. 81]

(4) EG II Movement During Percussive Damp Mode

(a) In the case $\overline{FU_4}$ is "1"

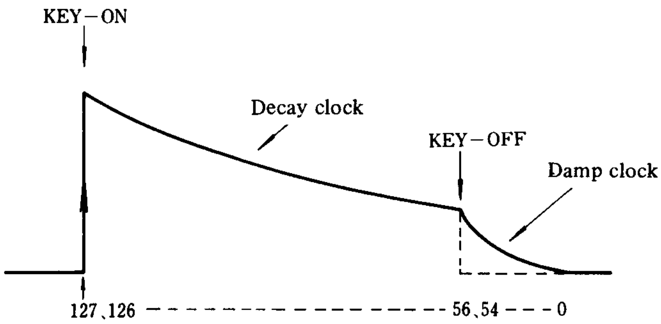
Normally this the same as the percussive, but when KEY OFF is set while it is decaying (subtractive counter in calculation) the counter is cleared at once to reach 0 step.



[Fig. 82]

(b) In the case $\overline{FU_4}$ is "0"

This is the same as the percussive mode during the key is being pressed, but when the key is released while it is decaying (subtractive counter in calculation) the decay clock is switched to another one and the counting is carried on with the decay clock. That is, from the very point the key is released, the damp clock fed out to $\overline{DAC}$ terminal is taken into EG II. The counter carries out the counting of the damp clock pulse from the value taken over to reach to 0 step.



This mode is used for vibraphone.

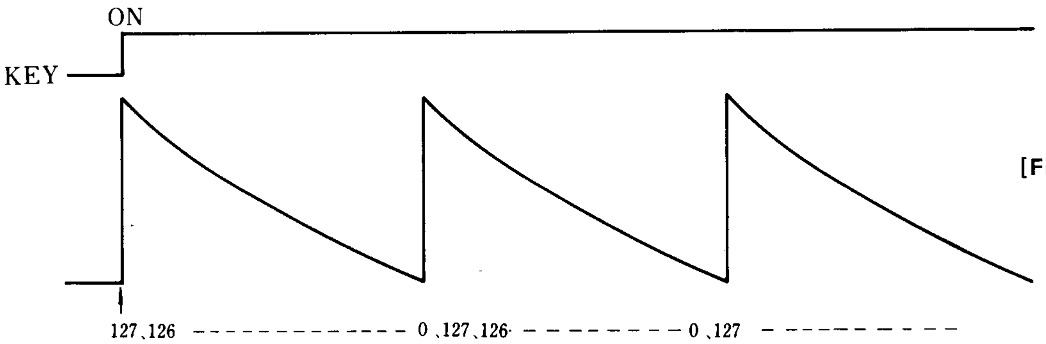
[Fig. 83]

(5) Attack Repeat Effect

The percussive repeat mode of Fig. 76 on page 55, as well as the percussive repeat damp mode, have the functions of watching the output condition of terminals $\overline{E_5} \sim \overline{E_{11}}$ within the IC of EG II, carring out self oscillation, and automaticaaly moving the counter again when the 0 address data appears.

This the same as the percussive mode, the Counter begins to count the decay clock pulse from 127 until 0 from the instant the key is depresse. The EG II is detecting the counting condition on the value detects "0".

With this data, the envelope control section set back the counter to "127" again and repeats this movement (127 → 0).

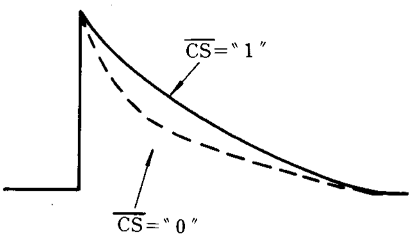


[Fig. 84]

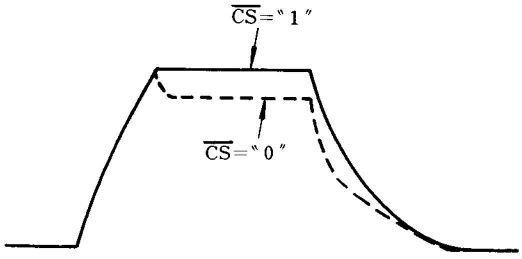
Naturally, the period of repeat can be varied by controlling the decay clock frequency.

7. Curve Select Terminals ($\overline{CUS}$, $\overline{CLS}$, $\overline{CPS}$)

This terminal is normally placed to "1" (≒ −15V) through the IC internal control, but when it is set to "0" forcefully from the outside, the output envelope wave form of EM changes as follows.

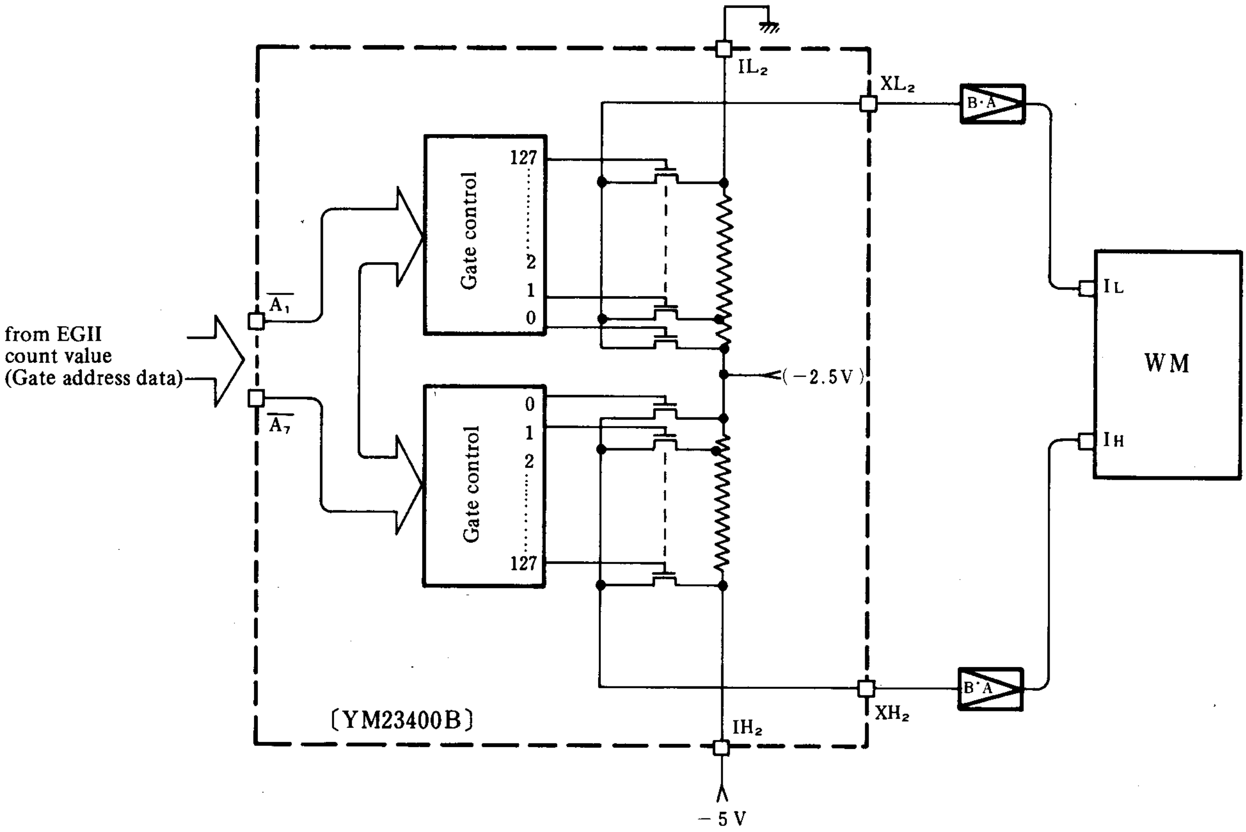


[Fig. 85]



This $\overline{CS}$ = "0" mode is utilized for only $\overline{CUS}$, $\overline{CLS}$ terminals of attack tone EG II.

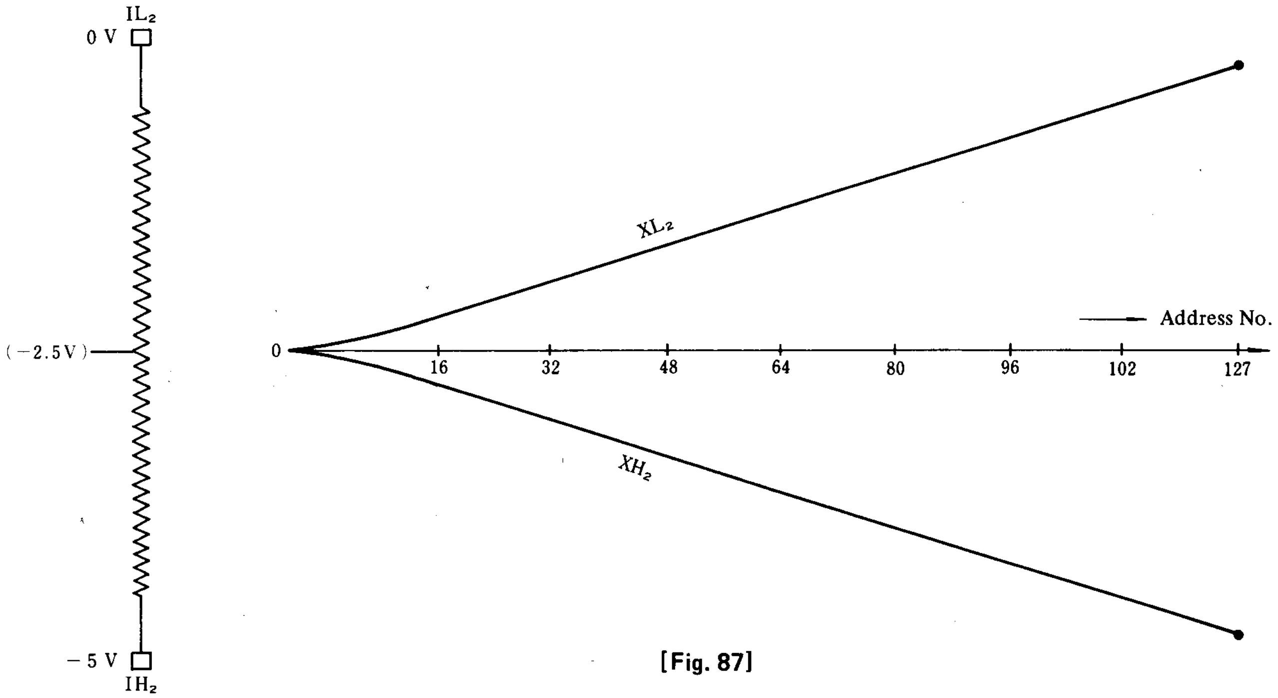
8. Principle of EM Movement



[Fig. 86] (Block Diagram of EM IC)

The EM carries out fines sampling mainly around −2.5V, within the IC between the IL_2· terminal (0V) and the LH_2 terminal (−5V); it is so constructed that each sampling voltage can be received through switching action.

This switching action is controlled by the 7-bit address code data sent from EG II. With the same address data it feeds a second value, mainly around −2.5V, to the XL_2 terminal, as well as to the XH_2 terminal.

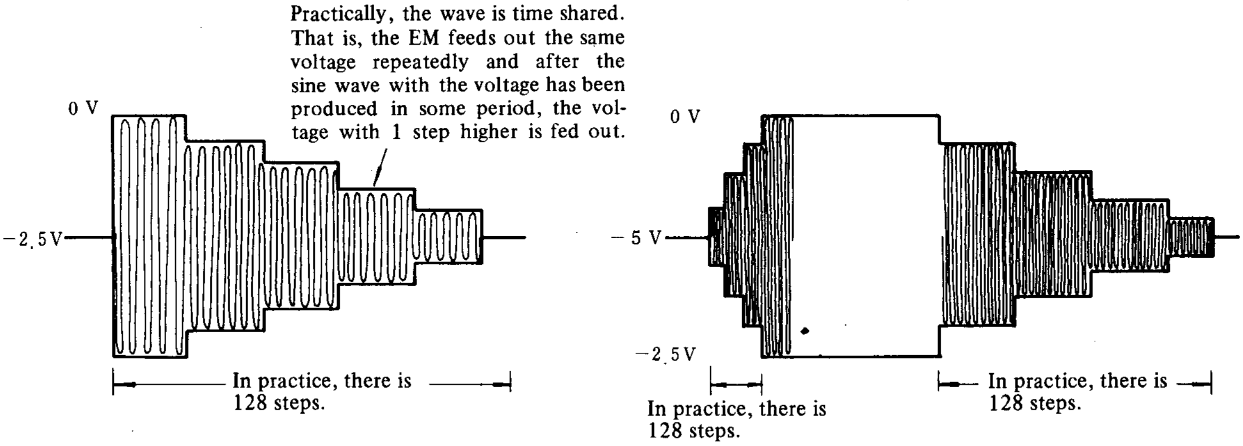


[Fig. 87]

The address data from EG II is sent at 1μS pulse width per channel and a 12μS frequency, so each sampling voltage is read out by each channel and added between terminals I_H and I_L of WM.

Therefore the oscillation width of the sine wave made by the EG changes in accordance with the output voltage from this EM.

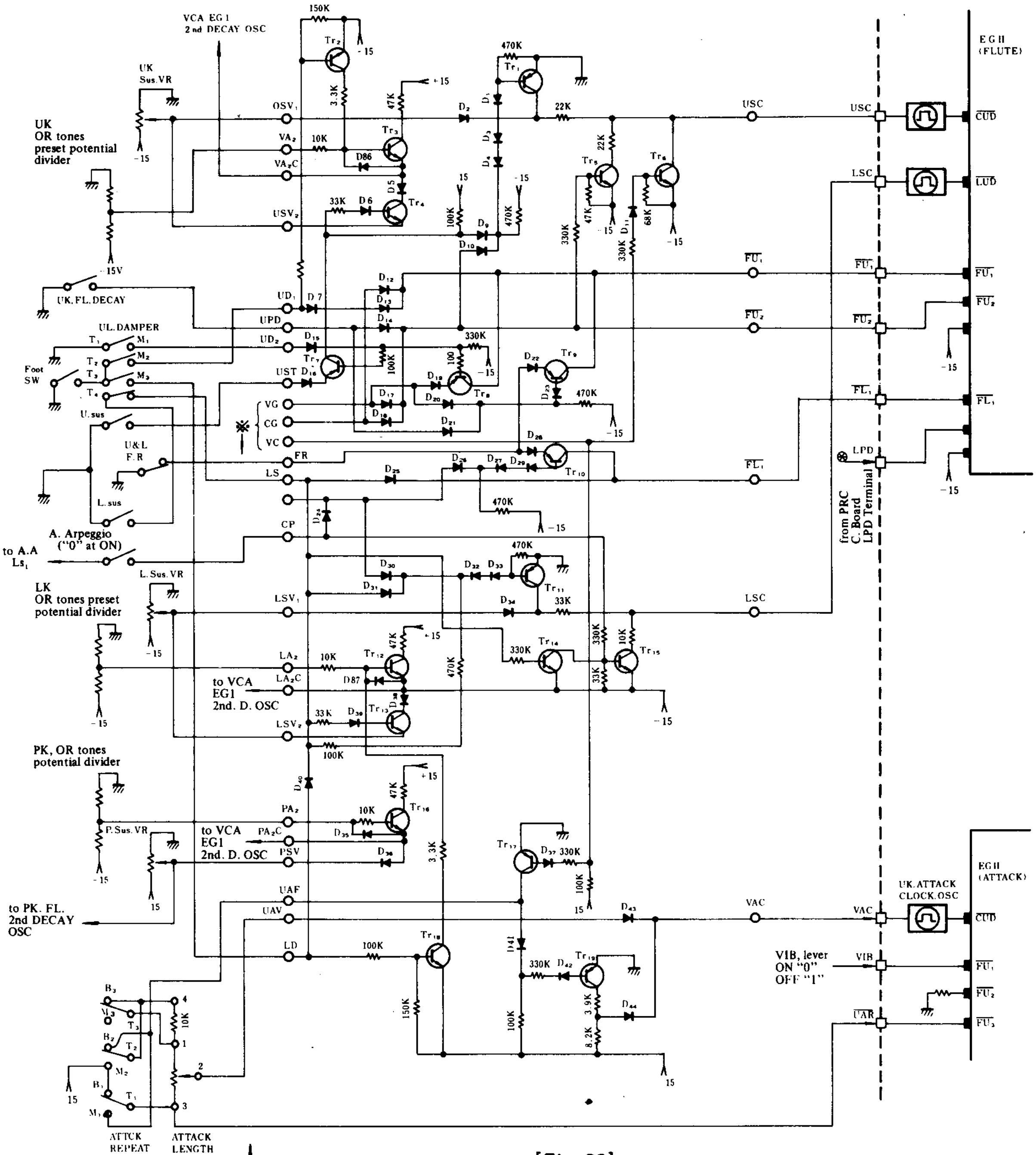
(Remarks) This change in the output sampling voltage from this EG is of sufficient time length, compared to the time for forming one frequency of the WM sine wave.



[Fig. 88]

9. The Envelope Control Movement of Flute Tones on E-70

PRC Circuit Board



	NORMAL	VIB	CHIMES
DG	1	0	1
CG	1	1	0
VC	1	0	0

[Fig. 89]

- **This is a explanation for the outline of the movement of Envelope Control Circuit for UK flute tone.**

(1) During NORMAL (All the effect tablets and levers are in NORMAL position)

(a) Since the envelope mode control terminals are in free condition except some terminals such as FR = 0V, VG = CG = VC ≒ −15V, the transistor Tr_1 is turned ON (−15V → 470K → D_4 → D_3 → Tr_1 Base). Tr_5 is in OFF condition and Tr_6 is in OFF to because −15V is given to VC terminal.
Due to the 0V (resulted from Tr_1 ON) is fed out to USC terminal, the oscillation frequency of the Decay Clock Generator for UK flute tone becomes highest and the decay time becomes shortest. (In this case, position of the Sustain Lever has no relation with this.)

(b) Tr_9 turns on with 0V of FR terminal and $\overline{FU_1}$ becomes "0". Also, as the other envelope control terminals are all in free condition, $\overline{FU_2}$ becomes "1" within the IC of EG II.

(c) The above results in that flute tone envelope is covered by Sustain mode during NORMAL and the decay time becomes shortest.

(2) In the case Sustain Tablet only is turned ON.

(a) Since the 0V is fed into the UST terminal, the Tr_7 turns on and D_4 becomes Cut-off condition through D_9.
Therefore, Tr_1 turns to OFF and the voltage of Sustain lever VR is fed out to USC terminal through D_2. This time, the decay time is controlled by Sustain lever.

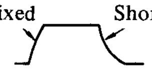
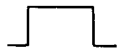
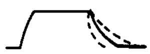
(b) $\overline{FU_1}$ and $\overline{FU_2}$ are, as the same as during NORMAL, set to "0", "1" mode namely the Sustain mode.

(3) In the case Flute Response Tablet only is turned on.
The FR terminal is shifted from 0V to free condition so that the Tr_9 turns OFF and $\overline{FU_1}$ turns to "1". $\overline{FU_2}$ is "1" as well, therefore, the mode becomes Direct Keying Mode.

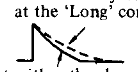
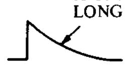
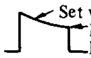
Switching of Envelope (Flute tone)

● U K **[Fig. 90]**

(Note) 0 ≒ 0 V, 1 ≒ −15V

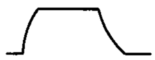
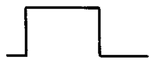
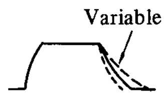
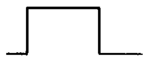
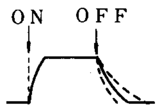
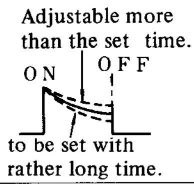
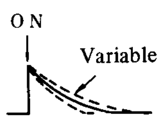
Condition	UK Flute Tone			
Tablet sw or lever sw turned on.	EGII Function Terminal Mode		Decay Time	Envelope Wave Form
	$\overline{FU_1}$	$\overline{FU_2}$	U S C	
NORMAL (only FR terminal is 0V)	0 (TR₉ ON with FR = 0V)	1	short (Tr_1 ON)	
FLUTE RESPONSE	1	1	———	
FLUTE RESPONSE + U & L DAMPER + FOOT SW	0 (D_7, D_{13} conducted)	1	Controlled by USV_1 (SUS, VR) voltage. (Tr_1 turns to OFF with D_7, D_9 conduction)	
DAMPER + F. SW (F·R is OFF)	0 (D_7, D_{13} conducted + Tr_9 ON)	1	〃	〃
U. SUS (U. SUS + K. S)	0 D_{13} is conducted (and Tr_9 ON with) Tr_7 ON.	1	Controlled by USVI terminal (SUS, VR) (Tr_1 turns to OFF with D_9 conduction)	
U. SUS (+K. S) + FLUTE RESPONSE	0 (D_{13} is conducted with Tr_7 ON)	1	〃	〃

(Note) 0 ≒ 0 V, 1 ≒ −15 V

Condition	UK Flute Tone			
Tablet sw or lever sw turned ON.	EGII Function Terminal Mode		Decay Time	Envelope Wave Form
	$\overline{FU_1}$	$\overline{FU_2}$	U S C	
U. SUS (+K. S) + U. FLUTE PERCUSSIVE DECAY	0 D_3 is conducted and Tr_9 turned on with Tr_7 ON	0 (D_{14} conducted)	Usually set to longer decay time. This can be further lengthen with USVI (SUS. VR)	SUS lever adjustable at the 'Long' condition.  Set with rather long even though the SUS lever is short.
U. FLUTE PERCUSSIVE DECAY	1 Tr_9 turned OFF with D_{21}, D_{23} conduction even FR is 0V.	0 (D_{14} conducted)	〃	〃 (to be Damp Mode)
U. FLUTE PERCUSSIVE DECAY +U.SUS(+KS)+DAMPER	1 Tr_7 turned OFF with D_{15} conduction	0 (D_{14} conducted)	〃	〃 (SUS is cancelled and becomes U.F.D.)
U.F.P.D+U.SUS(+KS) +DAMPER+F.SW	0 (D_7, D_{13} conducted)	1	Same as U.SUS +U.F.D	Same as U.SUU +U.F.D
U. SUS+DAMPER +F.SW	0	1	Same as DUPM +F.S	Same as DUPM + F.S
VIBRAPHONE (V G = 0 V) (V C = 0 V)	0 Tr_9 turned OFF with D_{20} conduction Tr_8 turned ON with D_{19} conduction.	0 (D_{17} conducted)	Set to the longest decay time (with VC terminal 0V, D_{11} conducted and Tr_6 turned on.	to be set with LONG 
CHIMES Lever (C G = 0 V) (V C = 0 V)	0 (D_{12} conducted)	0 (D_{18} conducted)	〃	〃
VIBRAPHONE +U.SUS	0	0	〃	〃
VIBRAPHONE +DAMPER (Same as SUS)	1 (Tr_8 O F F)	0	〃 (to be Damp Mode)	 Set with LONG Returns to with KEY-OFF.
VIBRAPHON +DUMPER +F.SW ((Same as SUS))	0 (D_7, D_{13} conducted)	0	Particulary for CHIMES lever same as ON	Particulary for CHIMES lever same as ON

(Note) • The $\overline{FU_3}$ terminal of EG II is fixed to "1" (−15V)
• The Attack Clock Generator for UK (common to LK) is set to fixed frequency (3 kHz).

● L K

Condition	LK Flute Tone			
Tablet sw or lever sw turned on.	EGII Function Terminal Mode		Decay Time	Envelope Wave Form
	$\overline{FL_1}$	$\overline{FL_2}$	U S C	
NORMAL only FR terminal is set to 0V	0 (Tr_{10} O N)	1	Short (Tr_{11} O N)	
FLUTE RESPONSE	1	1	———	
L. SUS (+K. S)	0 (D_{25} conducted)	1	Variable with LSV_1 terminal (sustain volume) Voltage (Tr_{11}, Tr_{15} OFF)	
L. SUS(+K. S) + DAM PER	1 (LS terminal opens)	1	Same as FLUTE RESPONSE	
L. SUS(+K. S) + DAMPER+F. SW	0 (D_{40}, D_{25} conducted)	1	Variable with LSV_1 terminal (sustain volume) voltage. (Tr_{11} turned OFF with D_{31} conduction and Tr_{15} turned OFF with Tr_{14} ON)	
Auto Arppegio Flute Tablet ON	1 Tr_{10} turned OFF with CP terminal "0".	0 (D_{24} conducted)	To be set with rather long time. further more controllable with Sustain volume. (Tr_{15})	
Auto Arpeggio Flute Tablet ON + L. SUS(+K. S)	0 (D_{25} conducted)	0	Controllable with LSV_1 terminal (Sustain volume) (Tr_{15} turned OFF with Tr_{14} ON)	

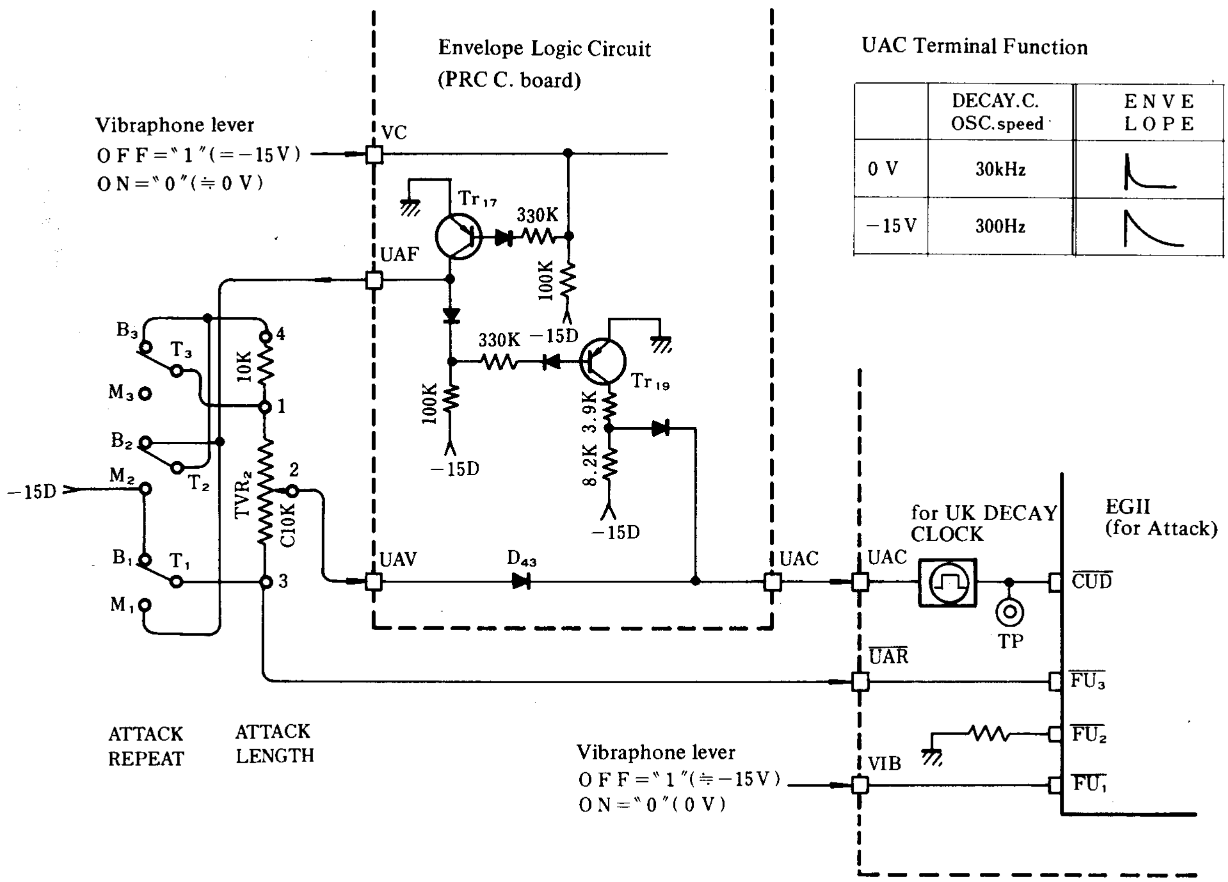
[Fig. 91]

(Remark) FL_3 terminal is fixed to "1".

● **UK Attack Tone Envelope Control**

The Wiring Block for Attack Repeat Effect Lever and EG II (for Attack)

• UK Attack Tone Envelope Control



	DECAY.C. OSC.speed	ENVE LOPE
0 V	30kHz	
−15 V	300Hz	

[Fig. 92]

The Wiring Block for Attack Repeat Effect Lever and EG II (for Attack)

(1) During NORMAL

(a) Tr_7 turns on and UAF terminal feeds out 0V
Tr_{19} turns OFF and D_{44} becomes CUT-OFF.

(b) The voltage 0V ↔ −15V is added to both ends of TVR_2 so that the divided voltage is fed out to the terminal UAC through D_{43} and controll the speed of Decay Clock OSC for UK.

(c) The terminals $\overline{FU_1}$ ~ $\overline{FU_3}$ becomes Percussive Damp Mode with "1", "0", "1".

(2) In the case Attack · Repeat Switch is turned ON.

(a) The opposite voltage from the preceding item (1) is added to the both ends of TVR_2. The more the TVR is forworded the more shorten the decay time.
Moreover, the terminal 1 of the TVR turns to be free condition and the voltage between 0 ~ −15V is divided by C10K (TVR_2) as well as 10K, therefore, the terminal 2 (UAV) of the VR_2 can not be −15V even it is in minimum and so, the maximum decay time becomes shorter than that of item (1).

(b) Consequently, the shorter the decay time becomes the faster the repeat speed becomes and that the Length Lever can identify the Repeat Speed Lever.

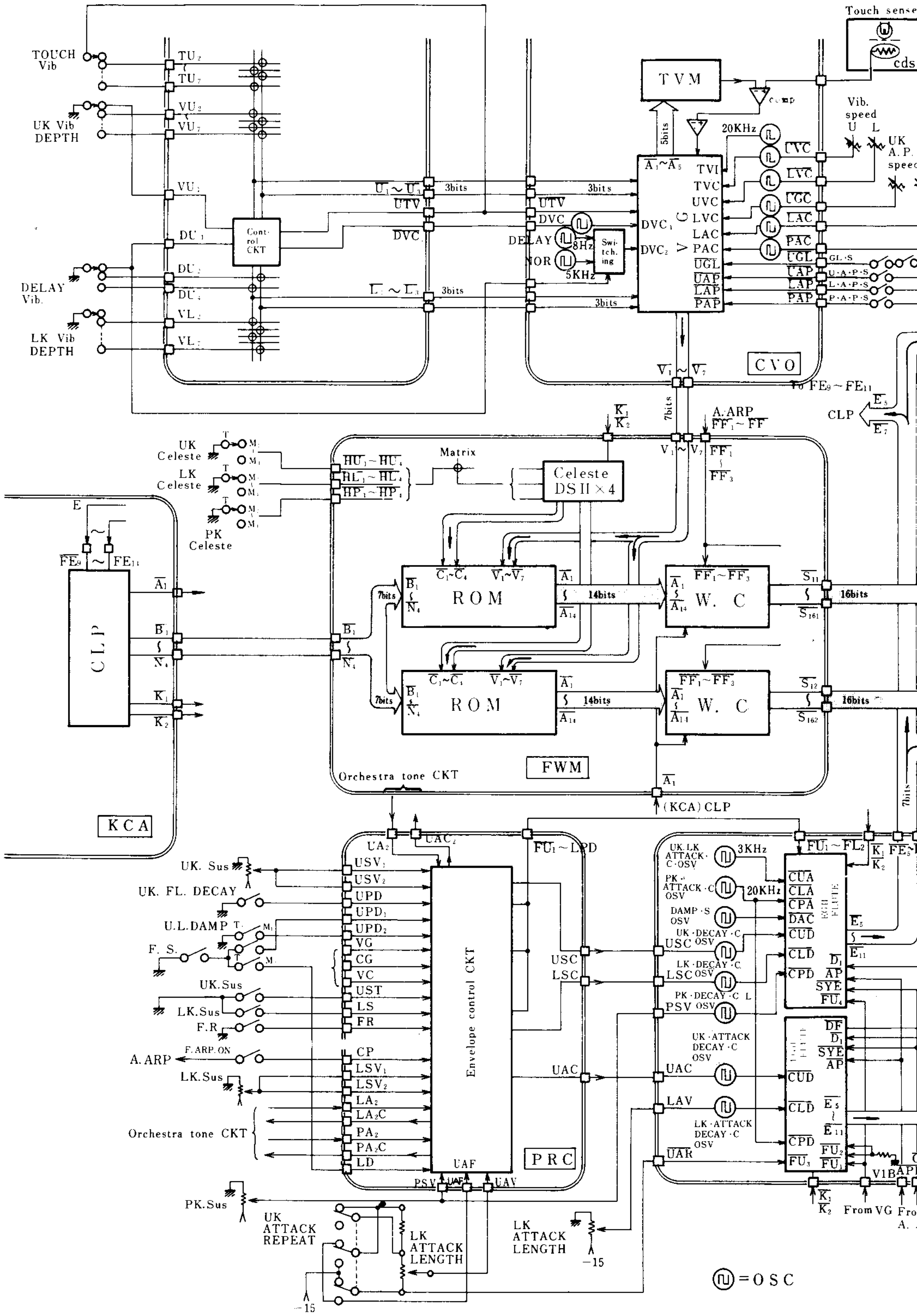
(3) In the case Vibraphone Lever is turned ON.

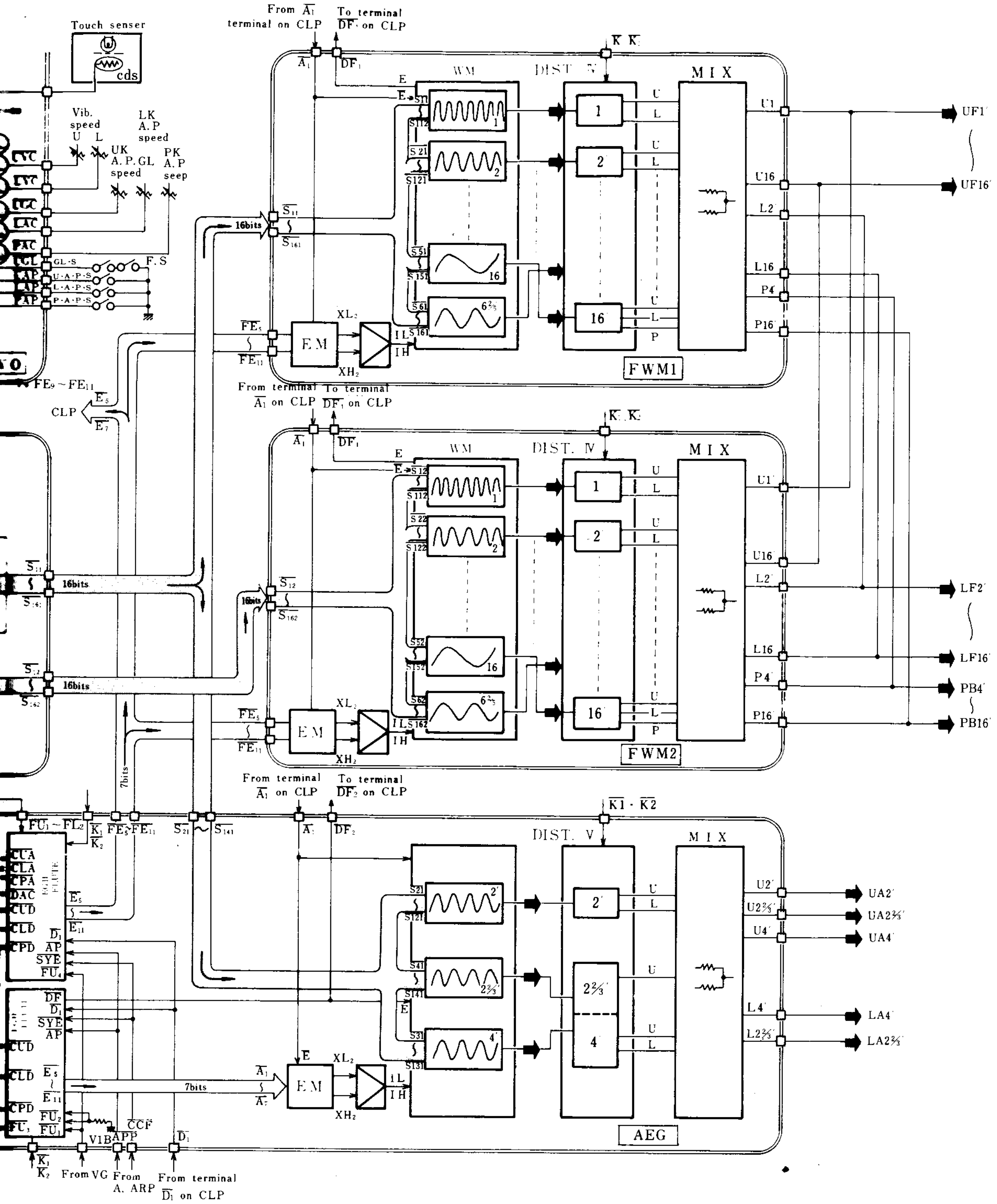
(a) Since Tr_{17} turns to OFF and UAF terminal becomes −15V, D_{43} turns to cut-off condition regardless of the position of Attack · Repeat · SW · TVR_2.
Still more, Tr_{19} turns to ON and feeds out the voltage (−4.8V) which is divided by the resistors 3.9K and 8.2K of the collector to UAC terminal through D_{44}. (Decay & Speed are fixed.)

(b) The terminals $\overline{FU_1}$ ~ $\overline{FU_3}$ turn to "0", "0", "1" of Percussive Mode.

- The envelope mode of LK attack tone is fixed to percussive mode and the decay clock is controlled by LK Length lever.
- The envelope mode of PK attack tone is fixed to percussive mode. The decay clock is used with flute tone and controlled by PK Sustain Volume lever.

PAS Basic Block Diagram




Touch senser
cds
Vib. speed
U L
LK A.P speed
UK A.P.GL speed
PK A.P seep
F.S
From A1 terminal on CLP
To terminal DF1 on CLP
K K
WM
DIST. IV
MIX
E
EM
XL2
XH2
IL
IH
U
L
P
U1
U16
L2
L16
P4
P16
UF1
UF16
FWM1
FWM2
16bits
7bits
FE9 ~ FE11
CLP
LF2
LF16
PB4
PB16
From terminal A1 on CLP
To terminal DF2 on CLP
K1 · K2
DIST. V
U2
U2⅔
U4
L4
L2⅔
UA2
UA2⅔
UA4
LA4
LA2⅔
AEG
FU1 ~ FL2
DF
D1
SYE
AP
CCF
V1B
APP
From VG
From A. ARP
From terminal D1 on CLP

C

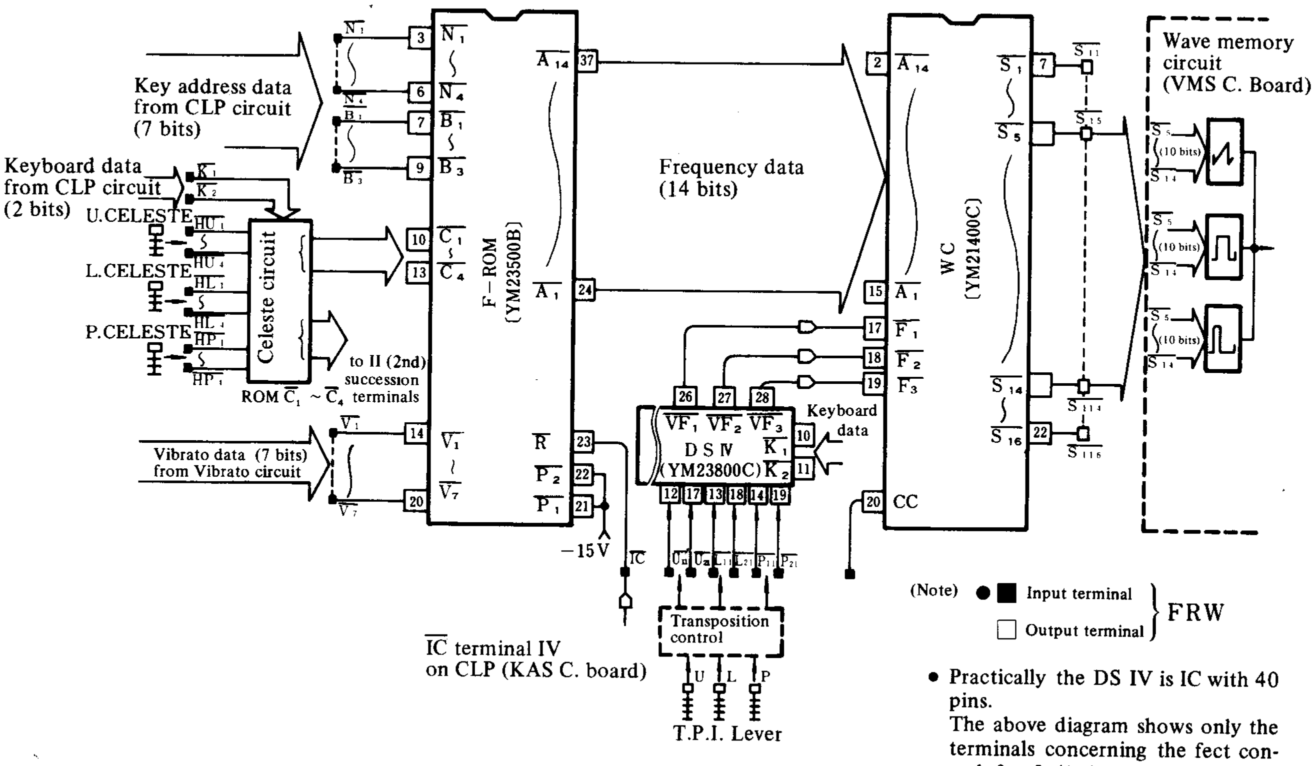
[Fig. 93]

5 ● FREQUENCY DATA GENERATION CIRCUIT II [PAS — VCF (ORCHESTRA TONES)]

1. Frequency Data Generation Circuit II

This circuit produces the frequency data to read out the wave form memorized in the Wave Memory Circuit (explained later) beforehand in accordance with the frequency corresponding to the key depressed.

The frequency data of this Circuit is of the same as that of flute tones, are produced with 12-sound time sharing by utilizing the key address data ($\overline{N_1} \sim \overline{B_3}$: 7 bits) from CLP circuit.



- Practically the DS IV is IC with 40 pins.
  The above diagram shows only the terminals concerning the fect control for I (1st) succession of the transposition lever.

(Basic Construction of Frequency Generation Circuit II) **[Fig. 94]**

2. Basic Construction of the Circuit

Consists of:

(1) Frequency-Read Only Memory (F–ROM)

(2) Wave Counter (WC)

and has the functions of Celeste and Vibrato.

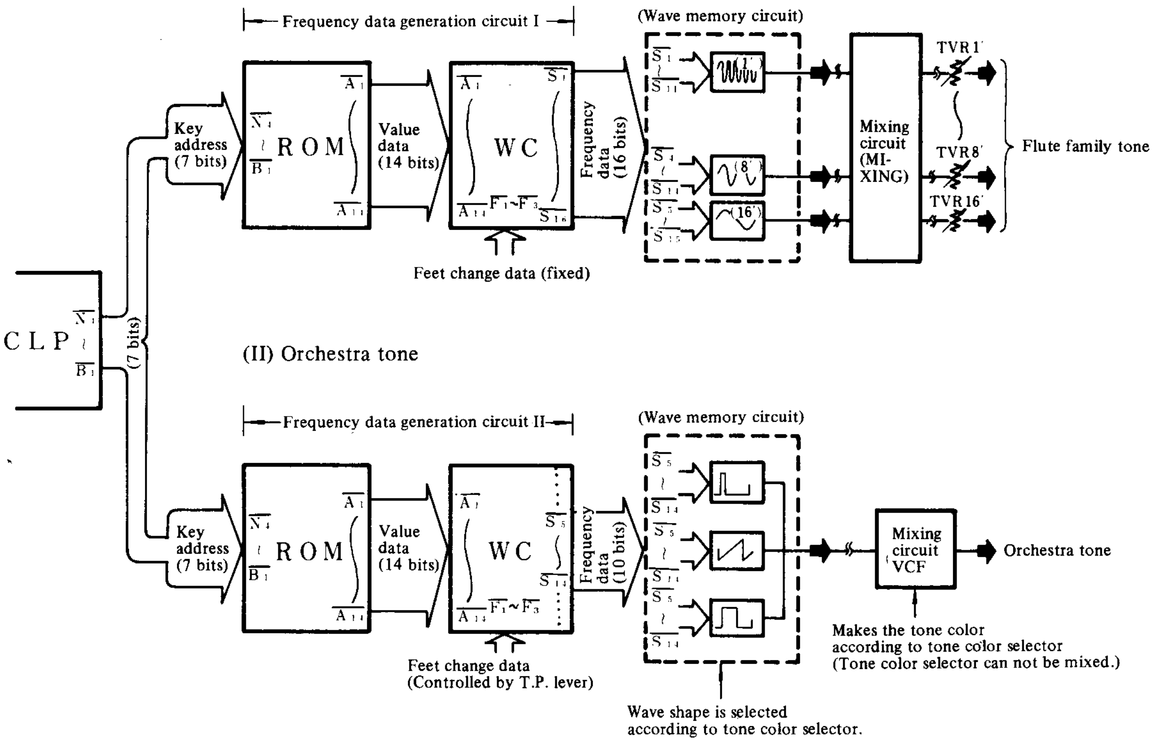
3. The Outline of the Movement of Frequency Data Generation Circuit II

- The principle of the movement of Frequency Data Generation Circuit II is quite the same as the Flute Frequency Data Generation Circuit I.
  The Orchestra tones, however, are produced by reading out the wave shape (⩘, ⎍, ⎍) with many overtones and adding the wave shape (tone source) to the voltage controlled filter.

- Therefore, contrary to the flute tone, the wave counter of the orchestra tone is not required to read out many waves related to overtone at the same time.
  Moreover, there is no need for making coupler tone since the mixing of these sound sources can not be carried out due to the method of filtering.

- For this reason, the orchestra tones take up only the 10-bit output data of $\overline{S_5} \sim \overline{S_{14}}$ terminals of Wave Counter to read out the wave shape for the tone source namely the frequency data.

- **Comparison of the Frequency Data Generation Circuit between Flute Tone and Orchestra Tone**



[Fig. 95]

(Note) The feet control terminals ($\overline{F_1} \sim \overline{F_3}$) are of the condition that Auto Arpeggio effect is in OFF.

4. Feet Switching Control for Orchestra Tone

In orchestra tones, as there is no need for making coupler tone at the same time, among the output (16 bits) of WC, only 10-bit of output data are adopted to read out the memorized wave shape. This results in the output frequency indicated by the data fed out from the terminal $\overline{S_{14}}$.

The feet change of orchestra tone, utilizing the feet control data ($\overline{F_1} \sim \overline{F_3}$: 3 bits) controlled by the TRANSPOSITION lever on the panel, can be carried out as follows.

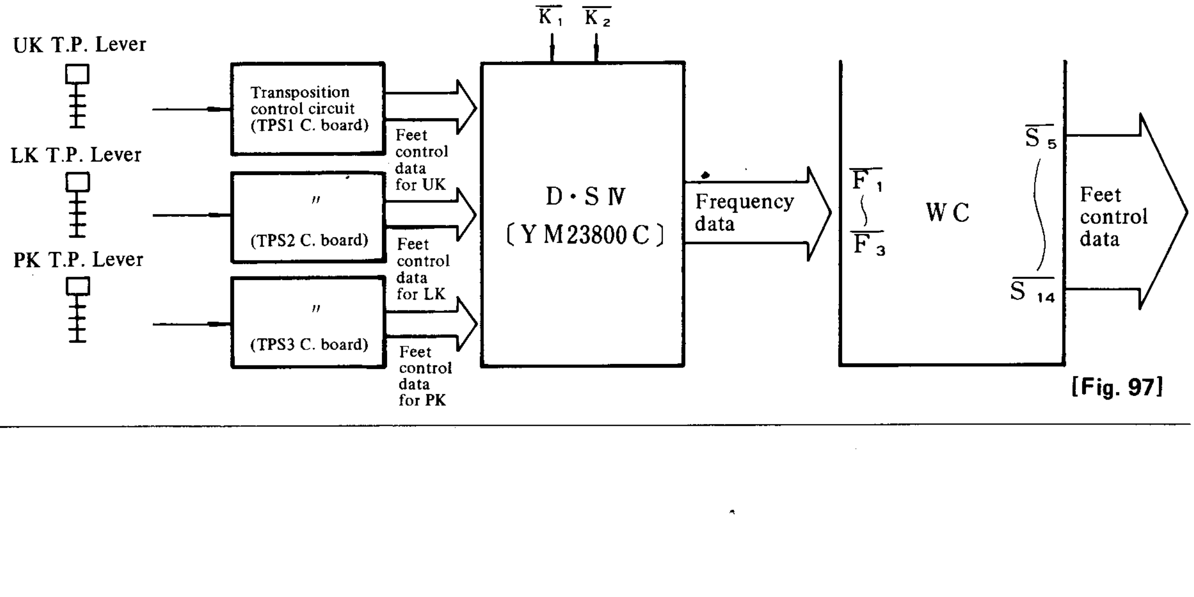
T.P Lever position	Octave switching terminal $\overline{F_1}$	$\overline{F_2}$	$\overline{F_3}$	Frequency indicated by each output terminal $\overline{S_5}$	$\overline{S_6}$	…	$\overline{S_{13}}$	$\overline{S_{14}}$	Frequency of tone source: Feet (Octave switching)
N	Set according to tone color			—	—		—	—	———
16	1	1	1	2^8f	2^7f		f	½ f	16′ (1 OCT DOWN)
8	0	1	1	2^9f	2^8f		2^1f	f	8′ (NORMAL)
4	1	0	1	2^{10}f	2^9f		2^2f	2^1f	4′ (1 OCT UP)
2	0	0	1	2^{11}f	2^{10}f		2^3f	2^2f	2′ (2 OCT UP)
				Output for interval frequency f.					

[Fig. 96]

(Note) 1. In T.P. Lever "N" position, "Feet" is determined in accordance with each tone color selector.
2. During Auto Arpeggio effect ON, the "Feet" is controoled by feet control data which is determinated by the effect.

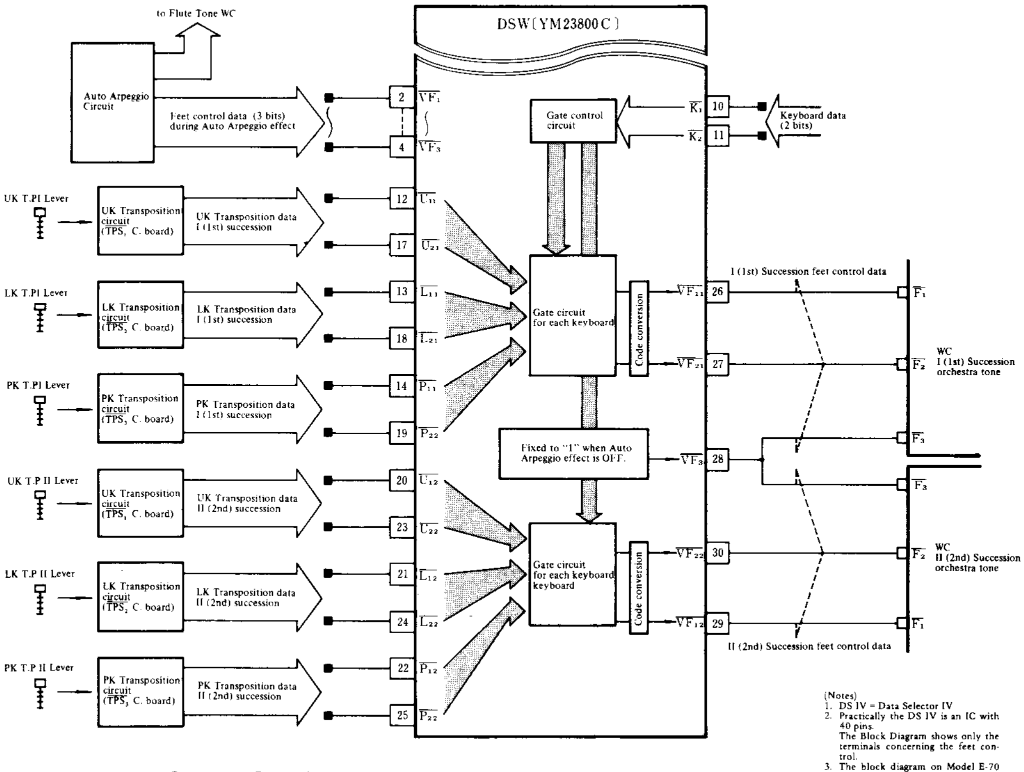
Moreover, the TRANSPOSITION levers are provided for each keyboard and according to the position of each lever, the feet control data are produced by Transposition circuit (TPS 1 ~ 3 circuit board).

The feet control data for each keyboard are controlled by DS IV (YM23800C) explained later, and added to the terminals $\overline{F_1} \sim \overline{F_3}$ of WC synchronizing with the channel of each keyboard.



[Fig. 97]

5. Feet Control Data Operation by DS IV (YM23800C)

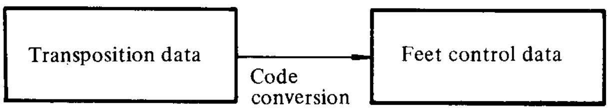


[Fig. 98] (Feet Control Data Operation by DS IV)

(1) Feet control by TRANSPOSITIONAL Lever (During Auto Arpeggio effect is OFF).

- The 2-bit Transposition data are fed into DS IV to control the "Feet" of Orchestra tone.
  The data are supplied for all keyboards simultaneously and changed by respective lever positions.

	DS IV Input-Output data				
T.P I Lever position	Input terminal mode		Output terminal mode		
UK Lever (LK Lever) (PK Lever)	$\overline{U_{11}}$ ($\overline{L_{11}}$) ($\overline{P_{11}}$)	$\overline{U_{21}}$ ($\overline{L_{21}}$) ($\overline{P_{21}}$)	$\overline{VF_{11}}$	$\overline{VF_{21}}$	$\overline{VF_{3}}$
N	※	※			
16'	1	1	1	1	1
8'	0	1	0	1	1
4'	0	0	1	0	1
2'	1	0	0	0	1



[Fig. 99]

(Notes)
1. "1" ≒ −15V
   "0" ≒ 0V
2. * marked are set to the following conditions by transposition circuit according to the tone color selector.
   - Set to 16'
     UK . . Trombone, Saxophone
     Jazz guitor,
     Electric guitor
     PK . . . Diapason, Bowed bass
     Funny II
   - Others are all set to 8'.
3. The data table depends upon the time when Auto Arpeggio is OFF. (Terminals $\overline{VF_1}$ ~ $\overline{VF_3}$ should be all "1".)
4. The control with T.P. II lever is the same as the above.

- DS IV detects the transposition data, synchronizing with the channel of each keyboard, by utilizing the keyboard data $\overline{K_1}$, $\overline{K_2}$.
  The detected data are converted to the code for feet control data. Then, the data of the 1st succession are fed out to the terminals $\overline{VF_{11}}$, $\overline{VF_{21}}$ while the data of 2nd succession to the terminals $\overline{VF_{12}}$, $\overline{VF_{22}}$ simultaneously.
  Moreover, when Auto Arpeggio effect is OFF, VF_3 (28 pin) is set to "1" within the IC and the terminal is used for both I and II successions in common.

- In this way, the feet of the tone created by time sharing is controlled by adding the feet control data to the WC octave switching terminals ($\overline{F_1}$ ~ $\overline{F_3}$)

(2) Feet Control during Auto Arpeggio effect is ON.

- The terminals $\overline{VF_1}$ ~ $\overline{VF_3}$ of DS IV is the input terminals for LK feet control data when Auto Arpeggio effect is ON.
  That is, the data detecting movement of DS IV is so constructed that it detects the input data of $\overline{VF_1}$ ~ $\overline{VF_3}$ in stead of LK transposition data when Auto Arpeggio effect is ON.
  Still more, the 3-bit feet control data taken with Auto Arpeggio effect are fed into these terminals from Auto Arpeggio Circuit Synchronizing with the LK channel time.

DS IV Input terminal			
$\overline{VF_1}$	$\overline{VF_2}$	$\overline{VF_3}$	Feet
1	1	1	16′
0	1	1	8′
1	0	1	4′
0	0	1	2′
1	1	0	1′

(Refer to the section of Auto Arpeggio.)

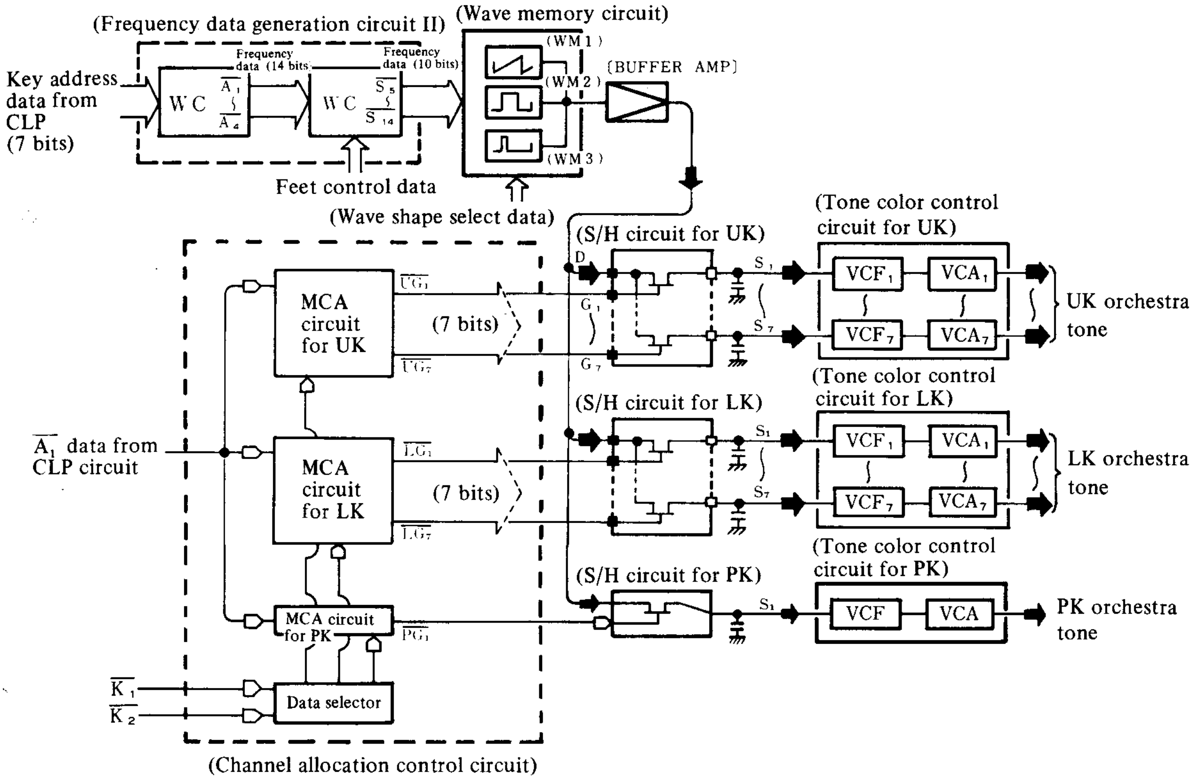
[Fig. 100]

(Notes)
- The data shown in the above table can be added to only when it is LK channel time.
- When Auto Arpeggio effect is OFF, $\overline{VF_1}$ ~ $\overline{VF_3}$ are all set to "1" so that the LK transposition data takes precedence.
- The UK and PK feet control are, regardless to Auto Arpeggio effect, controlled by TRANSPOSITION lever.

(Reference) In addition to the function of this feet control data, DS IV has also the function of interpolation data generation which controls the tone source wave form according to the range of note.

6 ● SOUND GENERATION CIRCUIT II [VCF SYSTEM]

- The Sound Generation Circuit II, which uses the voltage controlled filter (VCF) and voltage controlled amplifier (VCA), controlls the richness of overtones as well as the tone volume of tone sources (⩘, ⊓⊔, ⊓⊔) with time to produce many vivid sound. (The Orchestra Tone is a general tern for the sound produced by VCF system)
- That is, the Sound Generation Circuit II utilizes the frequency data ($\overline{S_5} \sim \overline{S_{14}}$: 10 bits) sent from the Frequency Data Generation Circuit II to read out a wave shape for an Orchestra tone source. (The principle is exactly the same as the Sound Generation Circuit I.)
  Since the VCF and VCA are provided with 7 circuits (for 7 tones) each toward UK and LK as well as 1 circuit (for single tone) for PK, the tone source signals can be allocated to each channel and controlled respectively.



[Fig. 101]

(Note) Envelope control section is excluded.

(Basic Block Diagram of Sound Generation Circuit II)

● Basic Circuit Construction

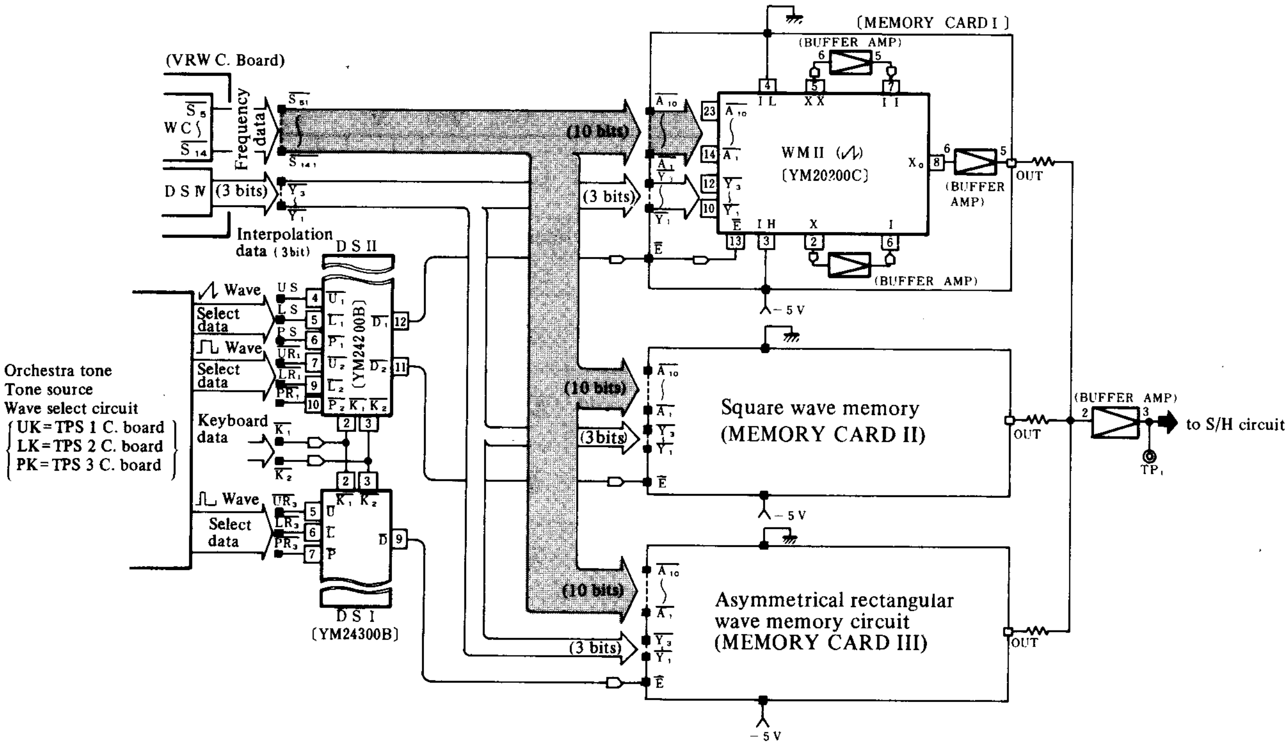
The circuit consists of:

(1) Wave Memory Circuit
(2) Channel Allocation Control Circuit
(3) Sample Hold (S/H) Circuit
(4) Voltage Controlled Filter and Amplifier (VCF, VCA)

6 — 1 • WAVE MEMORY CIRCUIT

1. Point

- This circuit memorizes three kinds of tone source wave form (⩘, ⊓⊔, ⊓⊔) for Orchestra tone into respective IC's and read out them according to the frequency of the key depressed by making use of 10-bit frequency data from the Frequency Data Generation Circuit II.
- The wave shape appointed to the tone color can exclusively read out.



[Fig. 102]

(Note)
- ▪ Input terminal / □ Output terminal — VMS C. Board
- Memory Card is equipped with VMS C. board
- A part of DS IC.
- PA611 (2 circuits of buffer amplifiers are built in.)

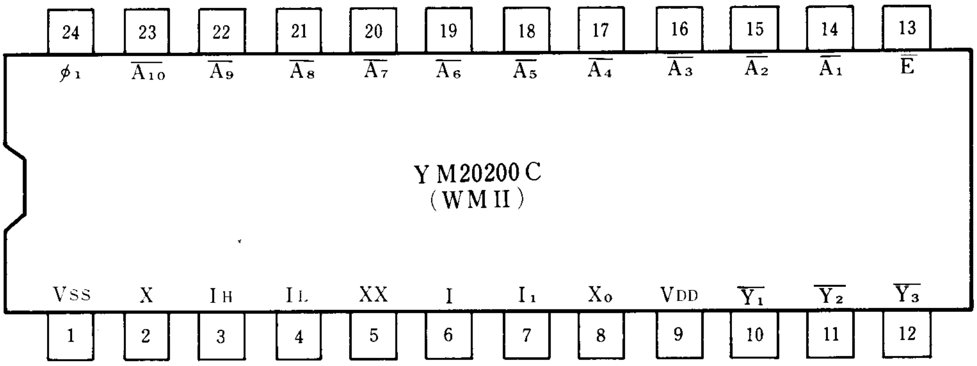
(Basic Construction of Wave Memory Circuit)

2. Basic Circuit Construction

- WMII (YM20200C: ⩘)
  Memorizes the Saw-tooth wave.
- WMIV−1 (YM20401B: ⊓⊔)
  Memorizes the Synmmetrical square wave
- WMIV−3 (YM240403B: ⊓⊔)
  Memorizes the Asymmetrical Rectangular wave

The basic circuit is so constructed with 3 kinds of Memory · Cords consisting of the above 3 IC's and also has the control circuit for Interpolation (wave shape control) and wave shape select.

3. YM20200C (WMII) Terminal Explanation



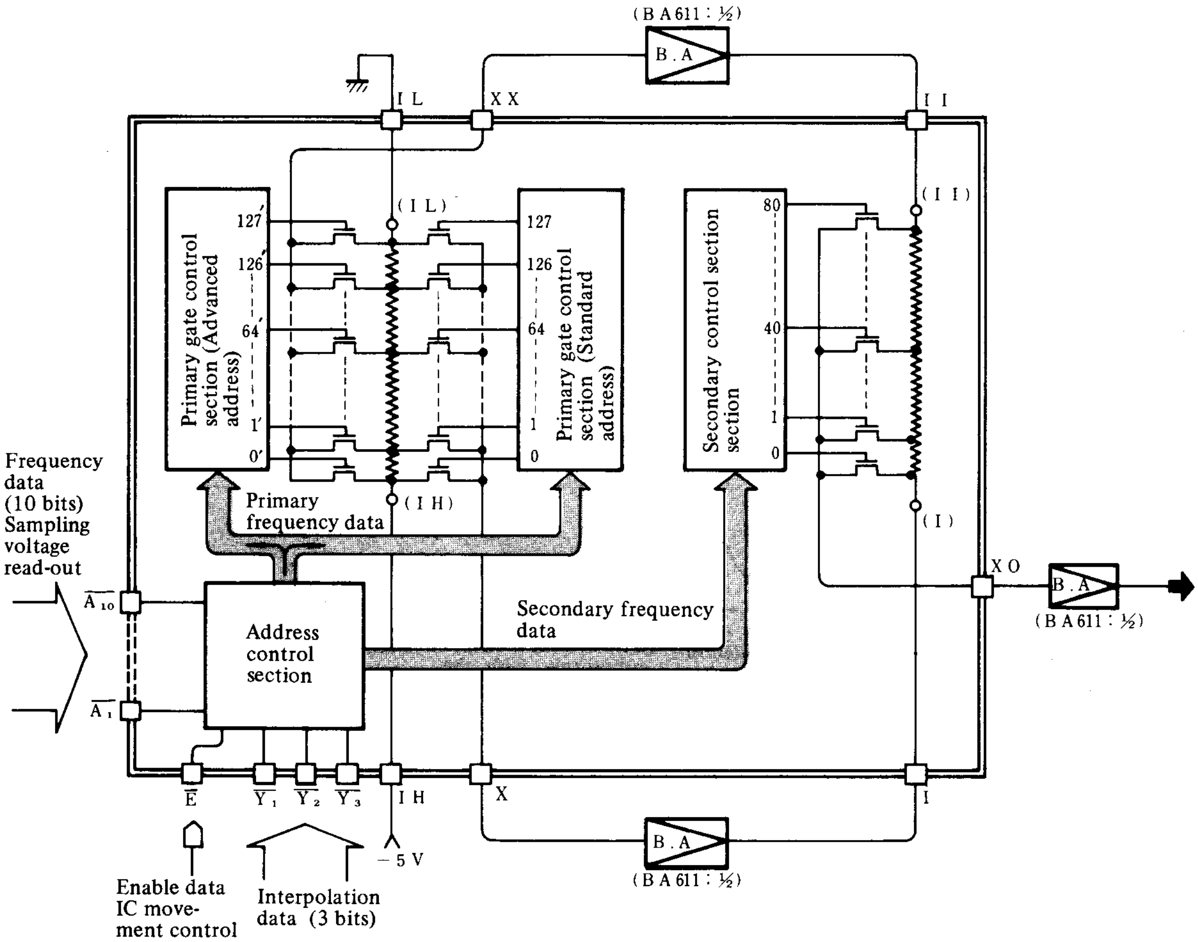
Terminal No.	Terminal Code	Designation	Significance	Terminal No.	Terminal Code	Designition	Significance
1	V_{SS}	———	Power source (0V)	24	∅1		Master clock (f ≒ 891 kHz)
2	X	———	Primary output 1 (To BUFFER AMP)	23	$\overline{A_{10}}$	———	Frequency data (Wave shape read out data) input terminals
3	I H	———	Input voltage for Amplitude (High) setting (−5V fixed)	22	$\overline{A_9}$	———	
4	I L	———	Input voltage for Amplitude (Low) setting (0V fixed)	21	$\overline{A_8}$	———	
5	X X	———	Primary output 2 (To BUFFER AMP)	20	$\overline{A_7}$	———	
6	I	———	Secondary input 1 (From BUFFER AMP)	19	$\overline{A_6}$	———	
7	I I	———	Secondary input 2 (From BUFFER AMP)	18	$\overline{A_5}$	———	
8	X O	———	Tone source wave shape output terminal	17	$\overline{A_4}$	———	
9	V_{DD}	———	Power source (−15V)	16	$\overline{A_3}$	———	
10	$\overline{Y_1}$	———	Interpolation data (3 bits) (Data to blunt wave shape more as the frequency getting higher.)	15	$\overline{A_2}$	———	
11	$\overline{Y_2}$	———		14	$\overline{A_1}$	———	
12	$\overline{Y_3}$	———		13	$\overline{E}$	Enable	IC Movement control terminal ("1" = OFF, "0" = ON)

(Note) Y M 20401 B (⊓L)
Y M 20403 B (ЛL) } are same as the above Table.

[Fig. 103]

4. Principle of WMII (YM20200) Movement

- The WMII, of the same as that of WMI for sine wave, obtaines the numerous sampling voltages which can be the momentary oscillation width of the wave. In other words, this IC divides the wave with time axis and also divides the voltage (voltage difference 5V fixed) between the terminals I_L and I_H.
  Moreover, the sampling voltages each are obtained by controlling the gates for respective sampling points. This Gate Control is carried out with 10-bit frequency data sent to the terminals $A_1 \sim A_{10}$ from WC.
- The 10-bit frequency data are divided into two groupes according to interpolation data ($\overline{Y_1} \sim \overline{Y_3}$: 3 bits), that is they are 7-bit primary frequency data (which controls the gates between the terminals I_L and I_H) and secondary frequency data (which controls the gates between the terminals I and II).



* [Fig. 104]

(Block Diagram of WMII IC)

- The Address Control Section divides the 10-bit frequency data ($\overline{A_1} \sim \overline{A_{10}}$) into two groupes – primary frequency data and secondary frequency data – according to the interpolation data ($\overline{Y_1} \sim \overline{Y_3}$: 3 bits)

Enable data	E="0"								$\overline{E}$="1"
Interpolation data (indicated by decimal notation)	0	1	2	3	4	5	6	7	
Primary frequency data (Controls the gates between the terminals IL and IN)	$\overline{A_{10}} \sim \overline{A_4}$	$\overline{A_{10}} \sim \overline{A_5}$	$\overline{A_{10}} \sim \overline{A_6}$	$\overline{A_{10}} \sim \overline{A_7}$	$\overline{A_{10}}$ $\overline{A_9}$ $\overline{A_8}$	$\overline{A_{10}}$ $\overline{A_9}$	$\overline{A_{10}}$		
Secondary frequency data (Controls the gates between the terminals I and II)	$\overline{A_3} \sim \overline{A_1}$	$\overline{A_4} \sim \overline{A_1}$	$\overline{A_5} \sim \overline{A_1}$	$\overline{A_6} \sim \overline{A_1}$	$\overline{A_7} \sim \overline{A_1}$	$\overline{A_8} \sim \overline{A_2}$	$\overline{A_9} \sim \overline{A_3}$		
Output wave shape	Few multiples ←→ Many multiples; Shape wave shape … Gentle wave shape							No output wave	

[Fig. 105]

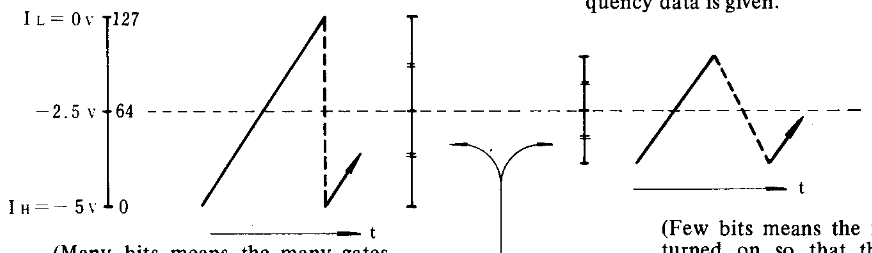
Like this, the primary and secondary frequency data are formed with respective bits of frequency data.

(Primary Read Out)

- The primary control section controls the gates between the terminals I_L and I_H by making use of the primary frequency data. The center voltage (–25V on gate address No. 64) is constantly maintained so that the gate control is carried out only to the direction from I_H to I_L.

(1) The order of gate movement when many bits of primary frequency data is given.

(2) The order of gate movement when few bits of primary frequency data is given.



(Many bits means the many gates are turned on so that the oscillation width of the read out wave becomes higher.)

Gate control is carried out always with the center voltage that is, –2.5V.

(Few bits means the few gates are turned on so that the oscillation width of the read out wave becomes lower.)

[Fig. 106]

There are two control sections for primary gates. They are the sections for Standard Address gates and advancing address gates. The advancing condition differs according to the number of bits.

[Fig. 107]

Primary frequency data (Number of bits)	$\overline{A_4} \sim \overline{A_{10}}$ (7 bits)	$\overline{A_4} \sim \overline{A_{10}}$ (6 bits)	$\overline{A_6} \sim \overline{A_{10}}$ (5 bits)	$\overline{A_7} \sim \overline{A_{10}}$ (4 bits)	$\overline{A_8} \sim \overline{A_{10}}$ (3 bits)	$\overline{A_9}$, $\overline{A_{10}}$ (2 bits)	$\overline{A_{10}}$ (1 bit)
Advancing condition (Standard address is assumed "0")	1	2	4	8	16	32	64

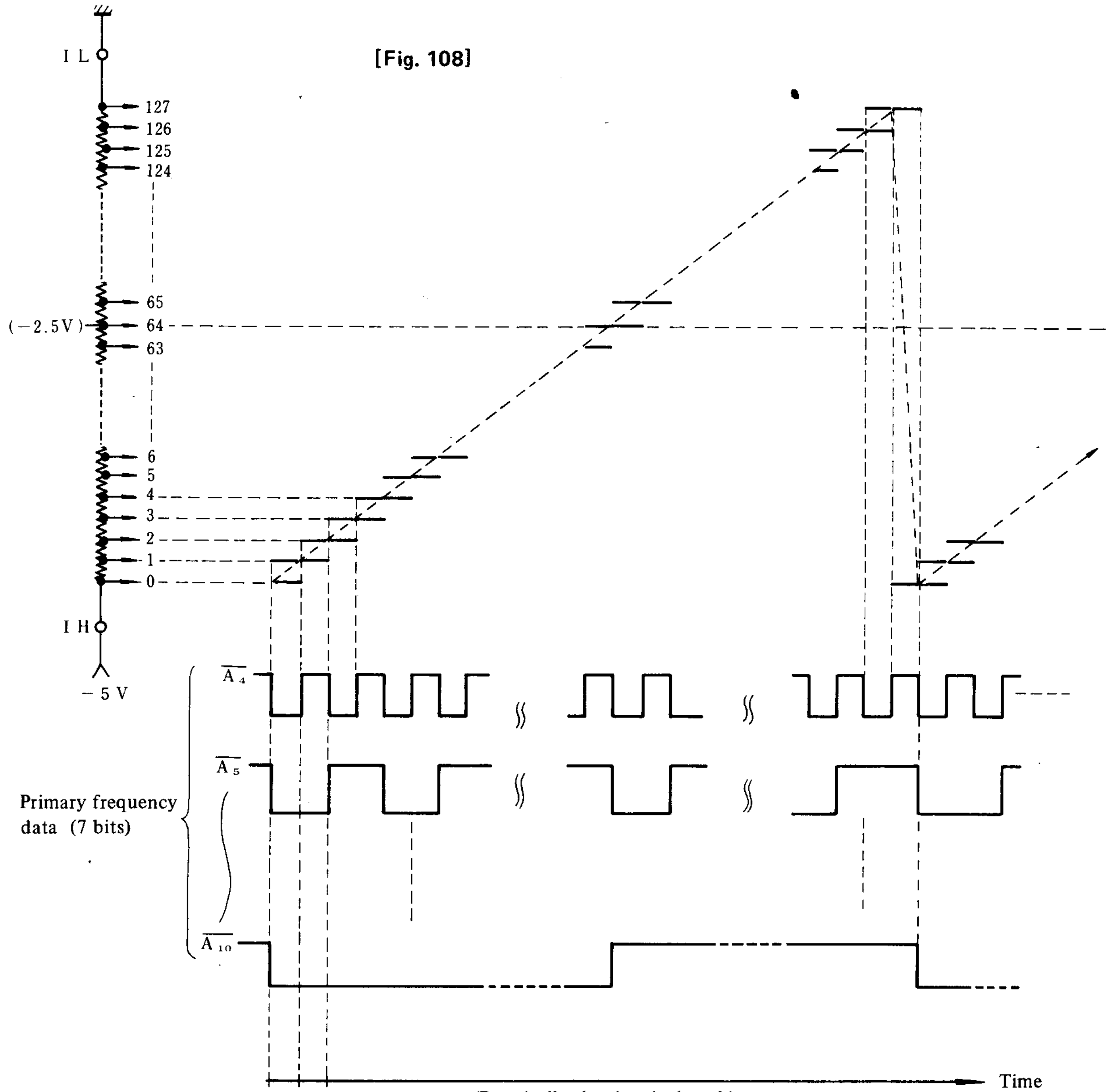
Therefore, two sampling voltages are read out at the same time, and fed out to X terminal and XX terminal respectively.

(Example) The output of the terminals X and XX (advancing condition is 1.) when primary frequency data are 7 bits ($\overline{A_4} \sim \overline{A_{10}}$).

(Remarks) —: X terminal output voltage (standard)

—: XX terminal output voltage (advance)

[Fig. 108]

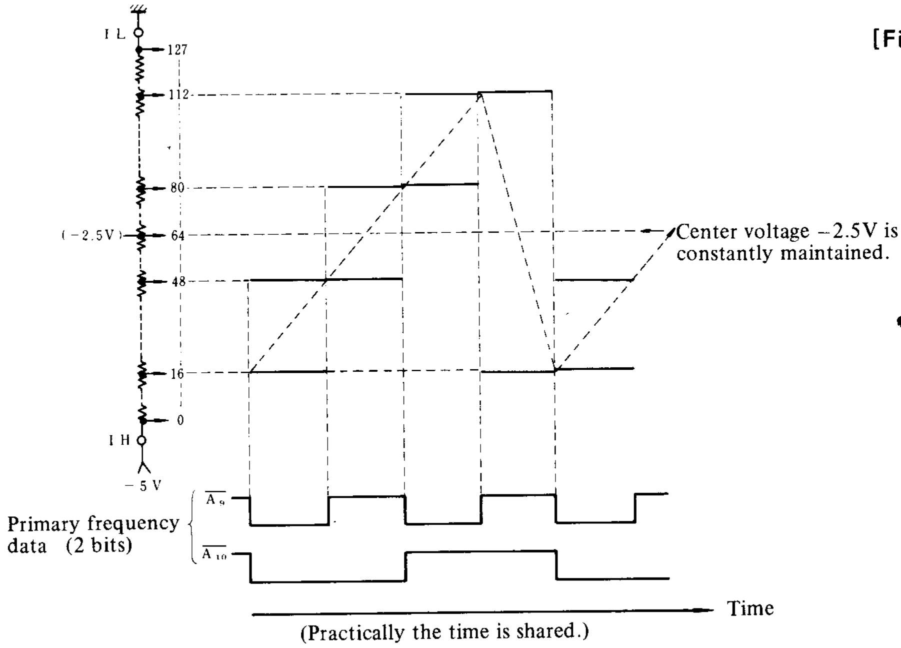


(Reference) 7 bits of primary frequency data operates 128 (2^7) gates within the time of one period (period for $\overline{A_{10}}$) of reading wave.

(Example) The output of the terminals X and XX (advancing condition is 32) when primary frequency data are 2 bits ($\overline{A_9}$, $\overline{A_{10}}$)

(Note) –: X terminal output voltage (standard)
–: XX terminal output voltage (advance)

[Fig. 109]



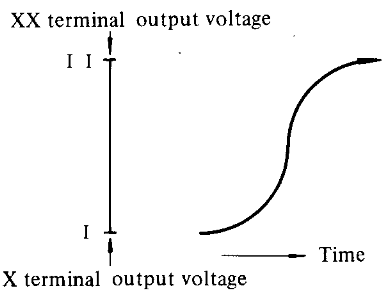
- The two sampling voltages read by primary frequency data are sent out to the terminals I and II through buffer amplifier.

(Secondary Read Out)

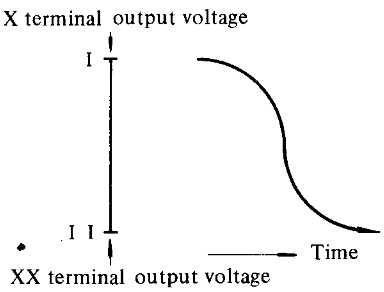
- The secondary gate control section controls the gates between the terminals I and II by utilizing the secondary frequency data. The gate control is carried out only to the direction from I to II, always contouring the one period of cosine curve.

(1) The order of gates movement when terminal voltage of II (XX) is higher than that of I (X).

(2) The order of gates movement when terminal voltage of II (XX) is lower than that of I (X).



[Fig. 110]

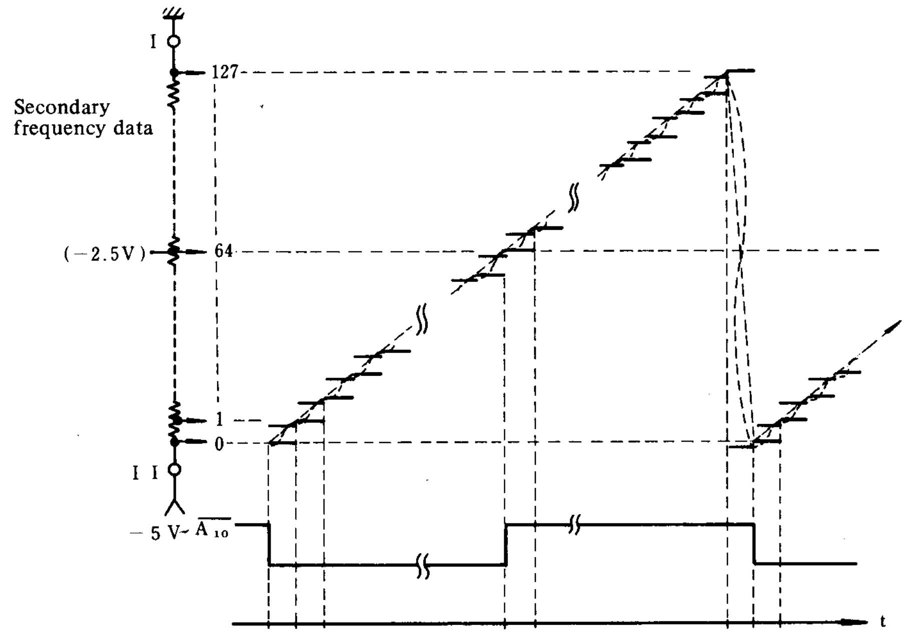


- That is, in this secondary reading section, the difference of two voltages read out by primary reading section are further finely divided. The finely divided voltages are read out according to the secondary frequency data so that the more smooth shape of tone source wave can be obtained.

5. WMII Output Example

(1) When the interpolation data value is 0.
Primary frequency data 7 bits ($\overline{A_{10}} \sim \overline{A_4}$)
Secondary frequency data 3 bits ($\overline{A_3} \sim \overline{A_1}$)

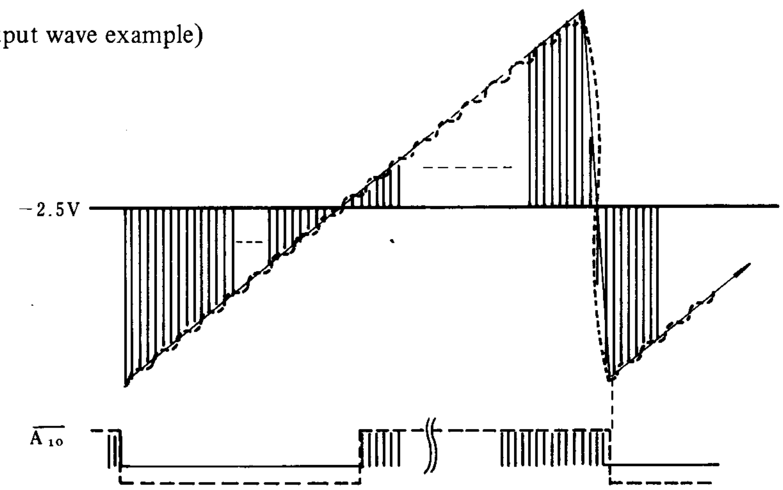
(Note) —: X terminal output voltage (I terminal input)
_: XX terminal output voltage (II terminal input)
/: XO terminal output voltage



(Practically the time is shared.)

[Fig. 111]

(Actual output wave example)



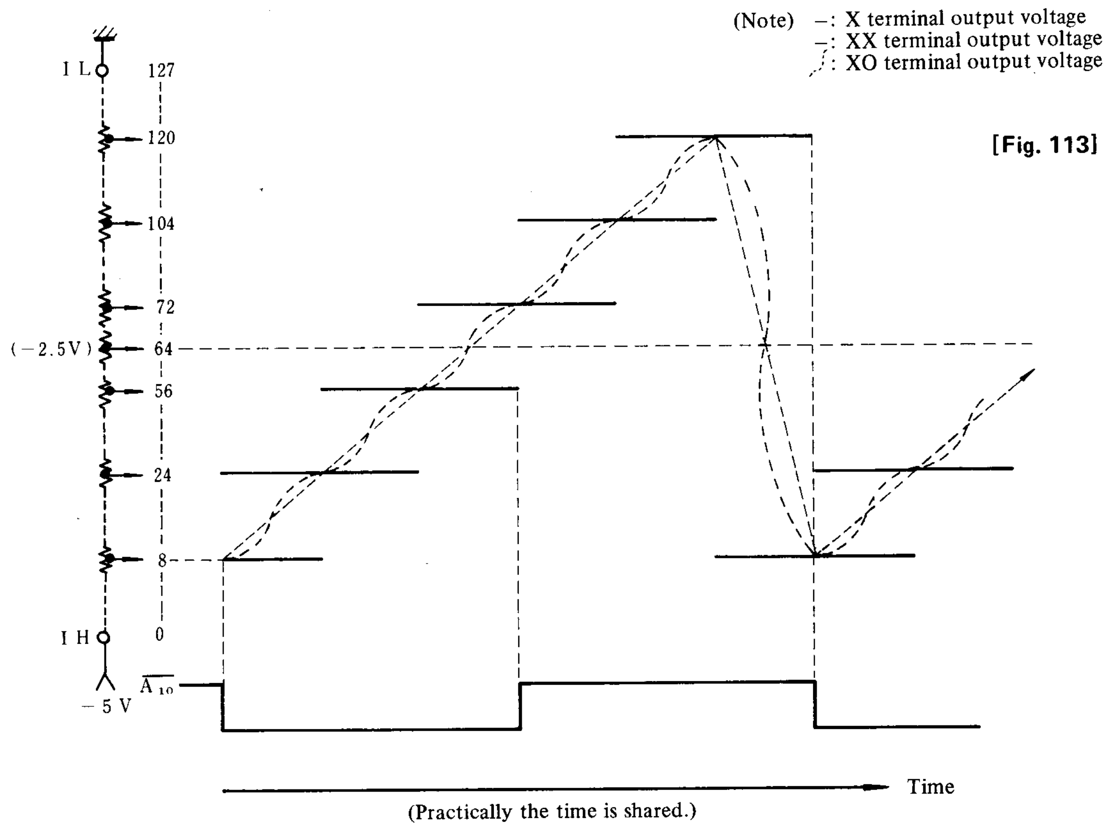
[Fig. 112]

(Reference) When interpolation data are up to 2 (0 ~ 2), the portion of the wave with sudden voltage change can distort.

(2) When interpolation data value is 4. (advancing condition 16)

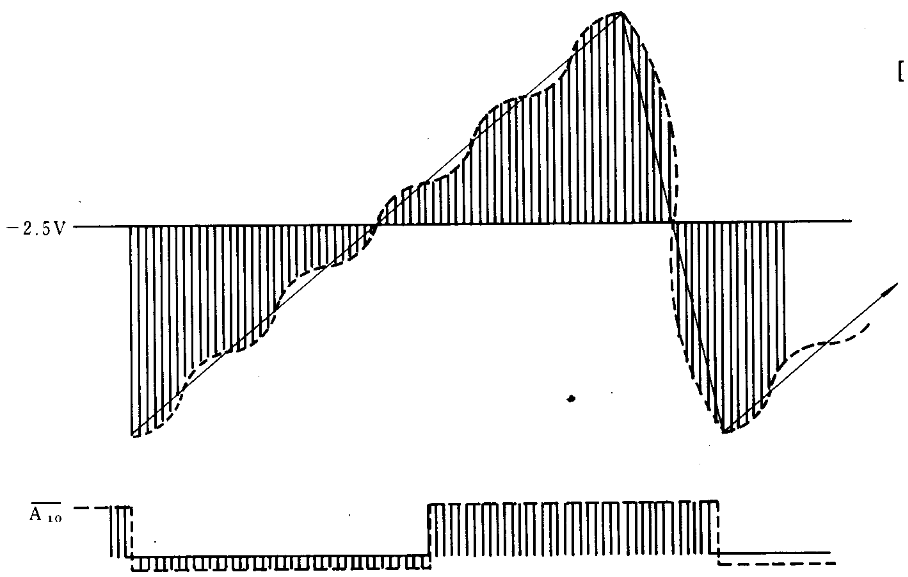
Primary frequency data 3 bits ($\overline{A_{10}} \sim \overline{A_8}$)

Secondary frequency data 7 bits ($\overline{A_7} \sim \overline{A_1}$)



[Fig. 113]

(Actual output example)

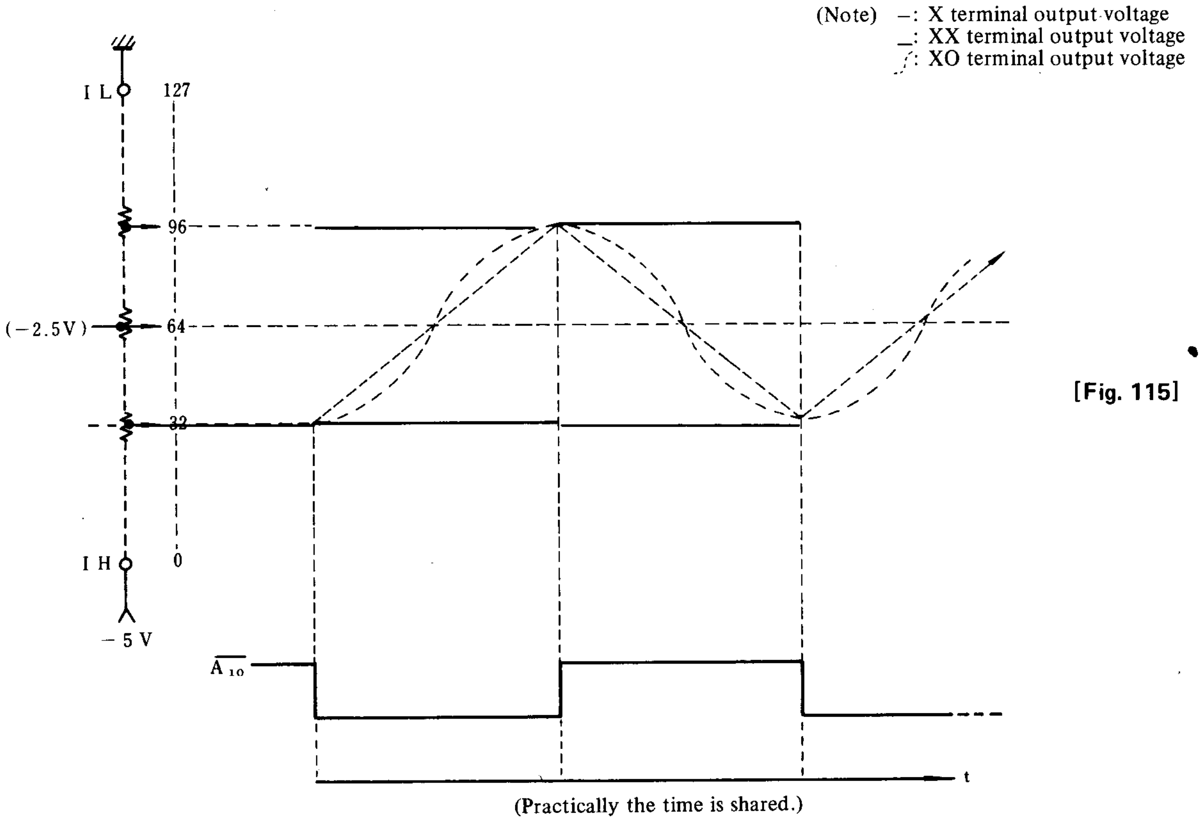


[Fig. 114]

(3) When interpolation data value is 6. (advancing condition 32)

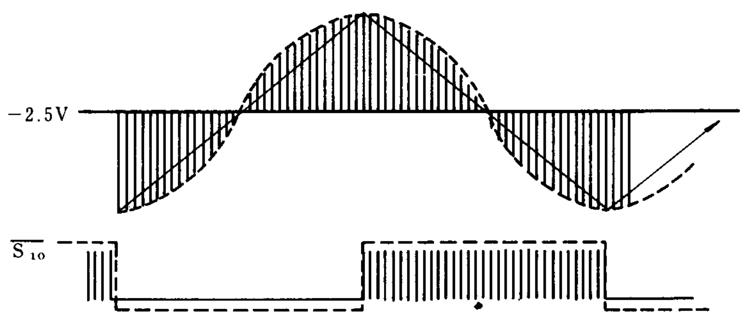
Primary frequency data 1 bit ($\overline{A_{10}}$)

Secondary frequency data 7 bits ($\overline{A_9} \sim \overline{A_3}$)



[Fig. 115]

(Actual output example)



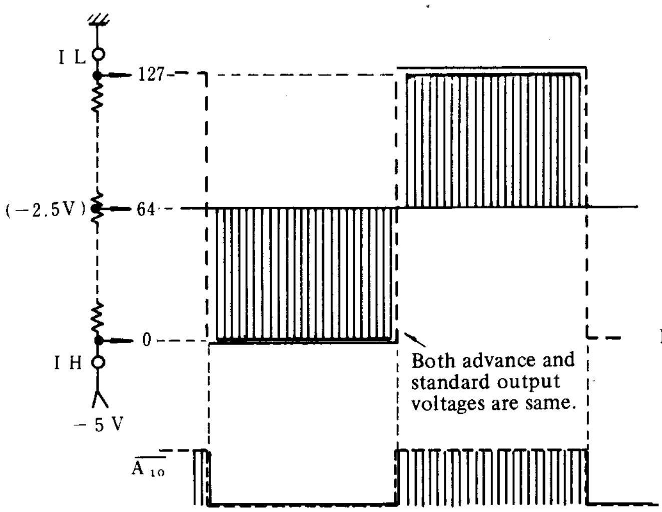
[Fig. 116]

6. Other WM Output Wave

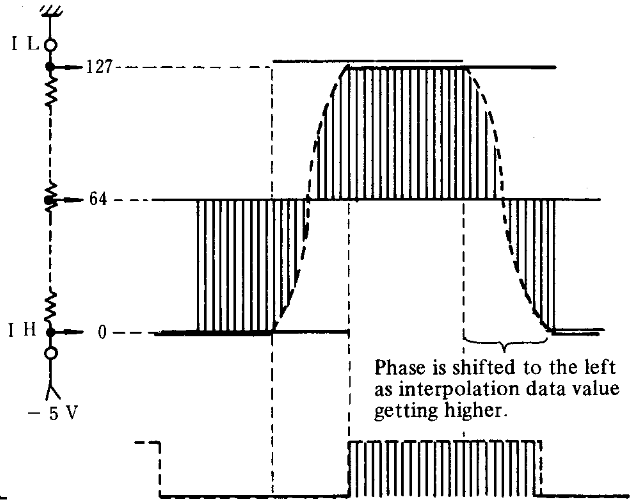
The WMIV–1 (YM20401B: for Square wave) and the WMIV–3 (YM20403B: for Asymmetrical rectangular wave) have the same movement as WMII, however, the advancing condition is concerned with the phase.

(Square wave output example) —: X terminal output voltage
–: XX terminal output voltage

(Interpolation data value = 0) (Interpolation data value = 5)



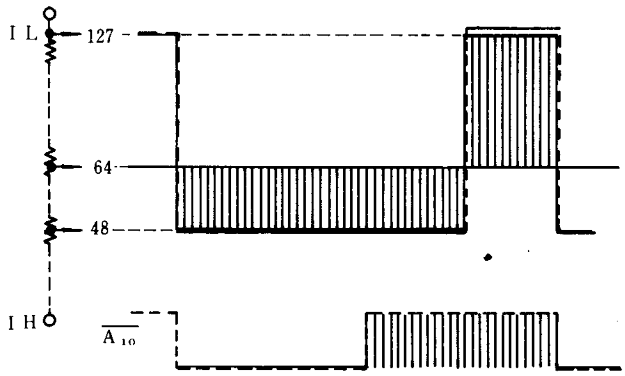
[Fig. 117]



[Fig. 118]

(WMIV–1 reads the only 2 values, namely I_L terminal voltage (0V) and I_H terminal voltage (–5V), from the voltage between I_L and I_H with primary frequency data.)

(Asymmetrical rectangular wave output example)
(Interpolation value = 0)



[Fig. 119]

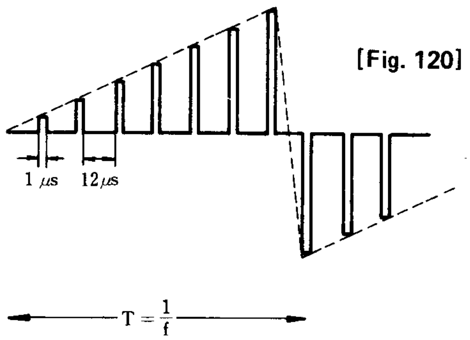
(WMIV–3 reads the only 2 values, namely the gate address No. 48 voltage and I_L terminal voltage (0V) from the voltage between I_L and I_H with primary frequency data.)

7. Interpolation Data ($\overline{Y_1}$ ~ $\overline{Y_3}$: 3 bits)

- The WM output wave (tone source signal) is produced through 12-sound time sharing so that the wave is formed with sampled voltages on the time axis. That is, the wave is modulated by sampling frequency ($\frac{1}{12\mu s} \doteqdot 83$ kHz).
- Of the waves read by the WM, those with a sharp fall contain overtone elements of a high order, therefore, the sampling frequences themselves and the overtones higher than arround one half of the sampling frequences interfer each other. For this reason, overtones with no relation to these sounds are generated. As a result, impure sounds are heard.

[Example] Consider the following WM output tone source wave shape.

(Tone source wave shape)

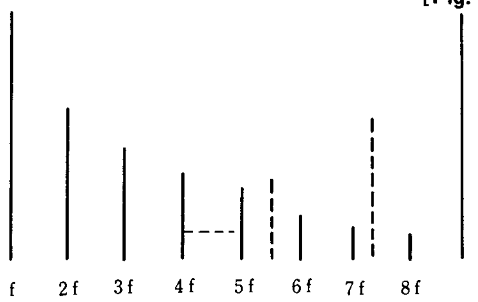


[Fig. 120]

(The more rise or fall of the wave sharpens, the higher overtones are contained.)

I: Overtone elements of sound source wave shape
I : Sampling frequencies (fs)
⁞ : Overtone elements of fs

(Overtone structure)

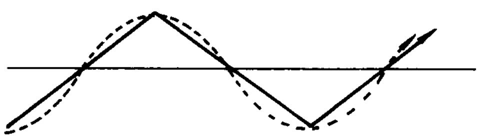


[Fig. 121]

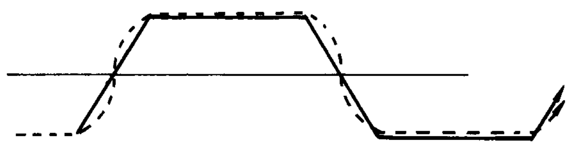
These overtones of the sound source are interfered with the sampling frequences and the frequences fs are generated. (This can refer to a kind of howling.)

- Then, to prevent the above phenomenon, interpolation data ($\overline{Y_1}$ ~ $\overline{Y_3}$: 3 bits) gentle the wave shape so that the wave may not contain the overtones higher than one half of the sampling frequences.

⇢ : With interpolation data
→: Without interpolation data



[Fig. 122]

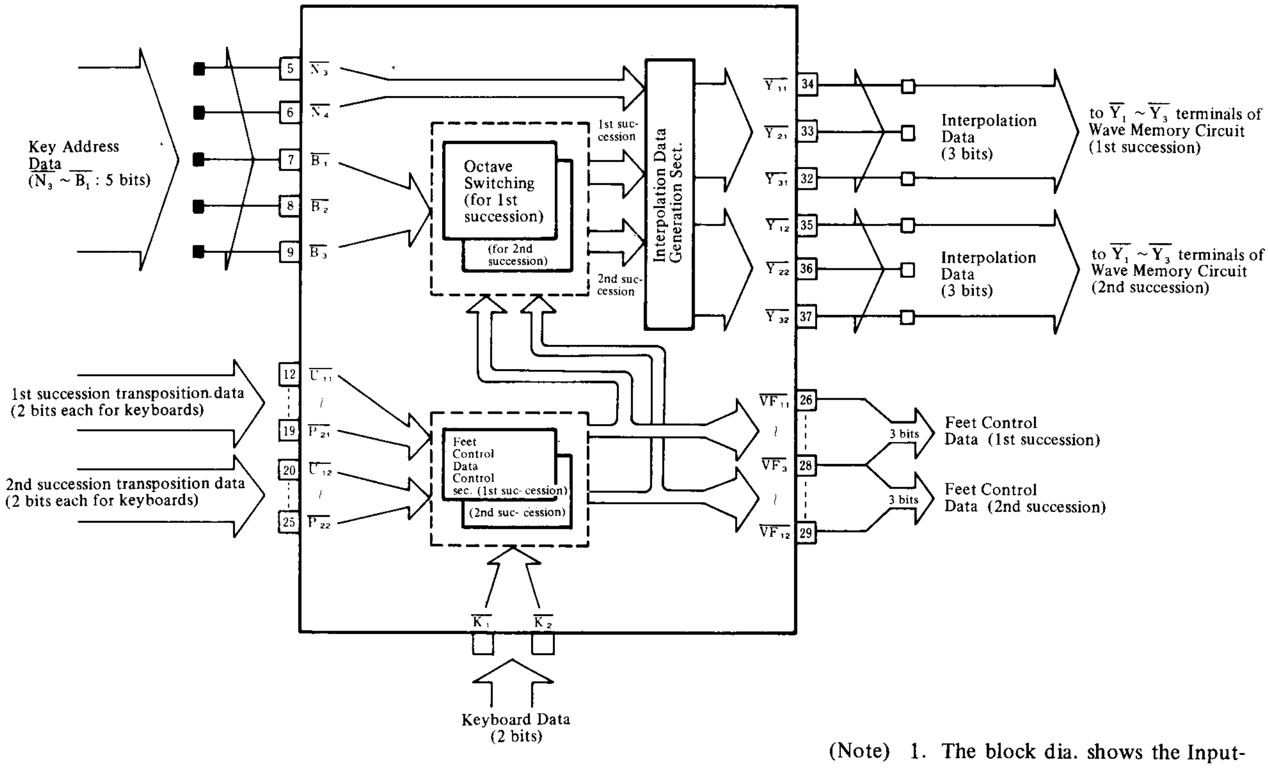


[Fig. 123]

Naturally, high frequency contains high overtones all the more, the interpolation data are so coded to control the wave shape according to the interval frequences.

- The value of this interpolation data are produced in conformity with the tone range by utilizing the key address data ($\overline{N_3}$, $\overline{N_4}$, $\overline{B_1}$, $\overline{B_2}$, $\overline{B_3}$) of DS IV (explained later).

8. The Principle of Interpolation Data Generation by DS IV



(Note) 1. The block dia. shows the Input-output of model E-70.
2. ■: Input terminal VRW
□: Output terminal C. board
3. Regarding the feet control data control section, refer to page 73.

[Fig. 124]

DS IV Basic Block Diagram

- The DS IV takes into the 5-bit data ($\overline{N_3} \cdot \overline{N_4} \cdot \overline{B_1} \cdot \overline{B_2} \cdot \overline{B_3}$) from among the key address data ($\overline{N_1} \sim \overline{B_3}$: 7 bits) fed out from CLP.
- Here, the key address data, regardless of the feet switching, indicates the key name (namely the tone name at 8') and are allocated to respective sounding channels.
- Therefore the Octave Switching section of this DS IV controls the octave data ($\overline{B_1} \sim \overline{B_3}$) so as to become the key address data in accordance with the feet of the TRANSPOSITION.
  The Octave Switching section discriminates the feet of the tone to be sounded in the channel time by using the output data from feet control data control section and according to it, switches the octave data which indicates the octave position of the key depressed.
- In this manner, the key address data with conversion of octive note are fed out to the interpolation data generation section so that the suitable interpolation data are generated.

[Interpolation Data]

[Fig. 125]

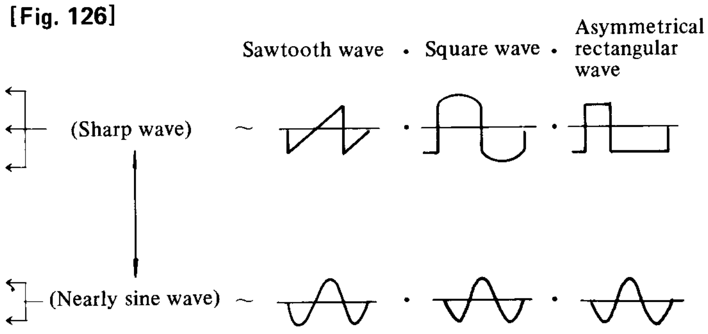
	$C_1 \sim D_2^{\#}$	$E_2 \sim A_2$	$A_2^{\#} \sim D_3^{\#}$	$E_3 \sim A_3$	$A_3^{\#} \sim D_4^{\#}$	$E_4 \sim A_4$	$A_4^{\#} \sim D_5^{\#}$	$E_5 \sim A_5$	$A_5^{\#} \sim C_6$
16′ (f/2)	0	0	0	0	0	0	0	1	2
8′ (f)	0	0	0	0	0	1	2	3	4
4′ (2 f)	0	0	0	1	2	3	4	5	6
2′ (4 f)	0	1	2	3	4	5	6	6	6

(Note) The above values indicate 3-bit interpolation data with decimal notation.

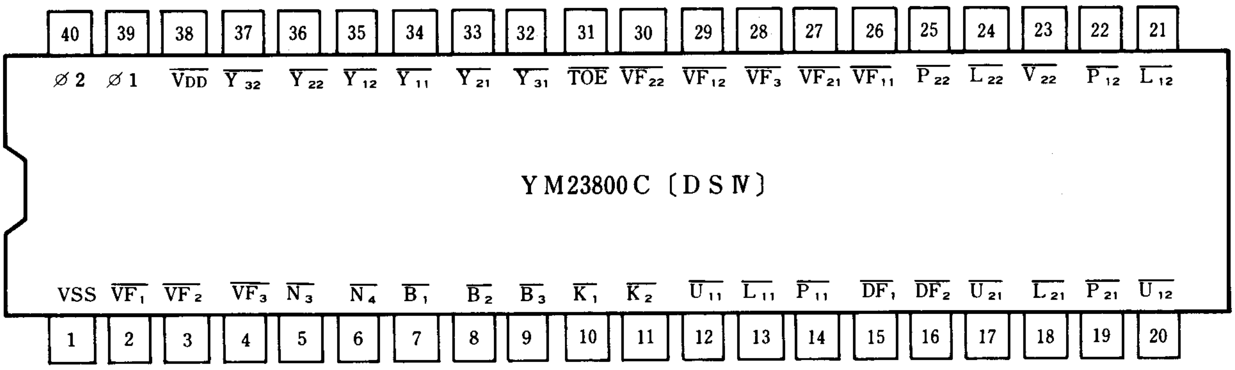
The relation between interpolation values and $\overline{Y_1} \sim \overline{Y_3}$. [Reference]

Terminal / Value	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$
0	1	1	1
1	0	1	1
2	1	0	1
3	0	0	1
4	1	1	0
5	0	1	0
6	1	0	0

[Fig. 126]



(Note)



[Fig. 127]

(Note) $\overline{TOE}$ = not used

With keyboard data ($\overline{K_1}$, $\overline{K_2}$), the DS IV (YM23800C) has the following functions.

(1) Selects the feet control data sent from the transposition circuit synchronizing with each keyboard channel and output to the WC terminals $\overline{F_1} \sim \overline{F_3}$. (Refer to page 73)

(2) Takes keyaddress data ($\overline{N_3}$, $\overline{N_4}$, $\overline{B_1} \sim \overline{B_3}$: 5 bits) into from CLP and produces interpolation data (3 bits) in accordance with the note range shown by the data.

9. Enable Terminal ($\overline{E}$)

There are three kinds of WM's, which memorize the different wave shape respectively, in the Orchestra tone wave memory circuit. Each WM moves with the "0" level of it's IC $\overline{E}$ terminal.

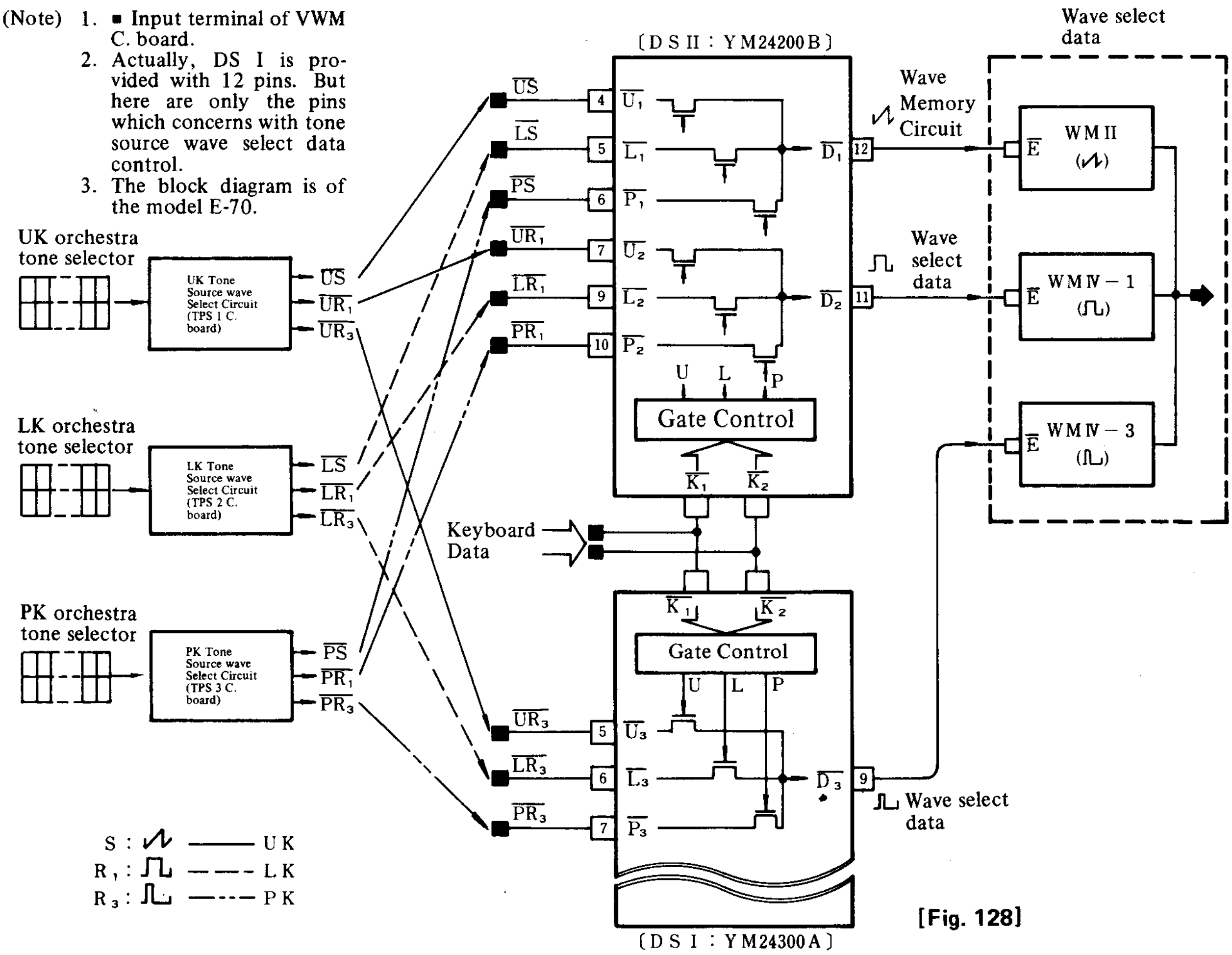
$\overline{E}$	WM
"0"	move
"1"	not move

Moreover, the terminal $\overline{E}$ of each WM is controlled in compliance with the tone selector of each keyboard so that the WM which memorizes the suitable tone source can be functioned.

10. Wave Select Control for Orchestra Tone Source

- The data (wave select data) to move three kinds of WM's (for Orchestra tone source, 、 、) are produced through the tone source wave select circuit (TPS 1 ~ 3 C. board) prepared for each keyboard.
- The wave shape select data for each keyboard are detected synchronizing with the channel time of each keyboard by DS I and DS II circuits and fed out to WM $\overline{E}$ terminal with this, WM can be controlled by tone selector of each keyboard.

(Note) 1. ■ Input terminal of VWM C. board.
2. Actually, DS I is provided with 12 pins. But here are only the pins which concerns with tone source wave select data control.
3. The block diagram is of the model E-70.

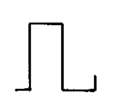
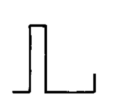


[Fig. 128]

Wave Shape Select Data Control by Data Selector

(The Principle of Data Selector Movement)

- The wave shape select data which conform with the tone selector are fed into the Data Selector in accordance with the keyboard.
- This Data Selector discriminates, by taking into the keyboard data ($\overline{K_1}$, $\overline{K_2}$), which keyboard tones are allocated to which channels.
- Based upon the discrimination, from among the wave select data of each keyboard being input in advance, it defects respective wave select data synchronizing with each channel time of each keyboard.

Input terminal	Output $\overline{K_1}$	Output $\overline{K_2}$	Output terminal	Select wave (WM)
$\overline{U_1}$	0	1		
$\overline{L_1}$	1	0	$\overline{D_1}$	
$\overline{P_1}$	0	0		
$\overline{U_2}$	0	1		
$\overline{L_2}$	1	0	$\overline{D_2}$	
$\overline{P_2}$	0	0		
$\overline{U_3}$	0	1		
$\overline{L_3}$	1	0	$\overline{D_3}$	
$\overline{P_3}$	0	0		

[Fig. 129]

(Note) Output becomes "0" only when the input is "0", and with this state each wave shape (WM) is selected.

(Example) When UK Clarinet tone selector button is pressed.
When a UK tone selector button is pressed, the voltages of the terminals $\overline{U_1}$, $\overline{U_2}$, $\overline{U_3}$ are determined respectively through UK wave shape select circuit (TPS 1 C. board).
That is, in case of clarinet, since the square wave is used as the tone source respective terminals become as follows. $\overline{U_1}$ = "1", $\overline{U_2}$ = "0", $\overline{U_3}$ = "1"
Therefore, "0" is fed out from $\overline{D_2}$ terminal during the channel time when keyboard data indicate the Upper Keyboard ($\overline{K_1}$ = "0", $\overline{K_2}$ = "1") with this, the WM for square wave moves simultaneously with the channel time.
In the same manner, LK and PK moves according to the setting condition of each tone selector.

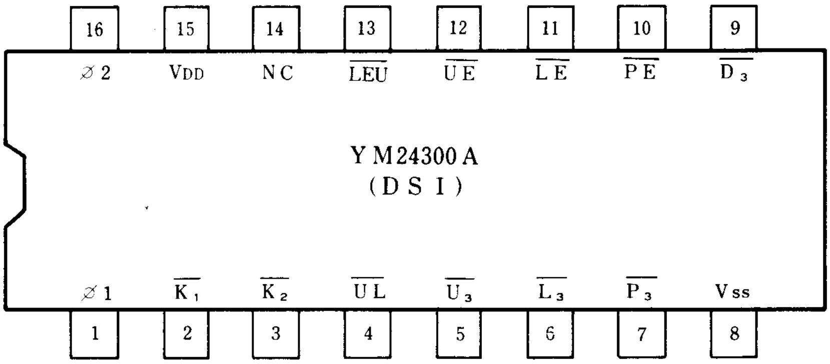
[Tone source wave shape for orchestra tones on model E-70]

Tone source wave shape \ Tone selector	UK	LK	PK
Sawtooth wave ($\overline{D_1}$="0")	Flute · Trombone Trumpet and other 8 tones	Flute · Trombone Horn and other 4 tones	Tuba · Trombone String Bass and other 5 tones
Square wave ($\overline{D_2}$="0")	Clarinet	————	Bass Clarinet •
Asymmetrical rectangular wave ($\overline{D_3}$="0")	Saxophone · Spring Electric Guitar · Funny II	Diapason · String Electric Guitar · Funny II	Diapason · Bowed Bass Funny II
Sawtooth plus Asymmetrical rectangular wave ($\overline{D_1}$=$\overline{D_3}$="0")	Piano · Jazz Guitar	Piano •	————

[Fig. 130]

(Reference)

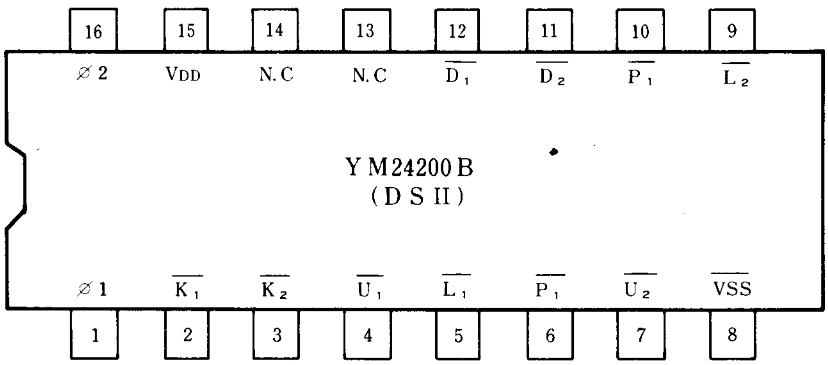
- DS I (YM24300A) Terminal Explanation



[Fig. 131]

Terminal No.	Terminal Code	Designation	Significance	Terminal No.	Terminal Code	Designation	Significance
1	∅1	Master clock	f ≑ 891kHz	16	∅2	Master clock	ϕ_2 is opposite phase from ϕ_1
2	$\overline{K_1}$	KEY BOARD DATA	Keyboard Data Input Terminal (2 bits)	15	VDD	———	Power source (= −15V)
3	$\overline{K_2}$	〃		14	NC	———	not used
4	$\overline{UL}$	UPPER PLUS LOWER	UPPER PLUS LOWER Effect switch connection terminal ("0" = ON)	13	$\overline{LEU}$	LOWER and UPPER ENABLE	Enable data output terminal for LK · MCA
5	$\overline{U_3}$	UPPER	⎍ Wave select data input terminal by keyboard	12	$\overline{UE}$	UPPER ENABLE	Enable data output terminal for UK · MCA
6	$\overline{L_3}$	LOWER		11	$\overline{LE}$	———	not used
7	$\overline{P_3}$	PEDAL		10	$\overline{PE}$	PEDAL ENABLE	Enable data output terminal for PK · MCA
8	Vss	———	Power source (= 0V)	9	$\overline{D_3}$	———	⎍ Wave select data output terminal

- DS II (YM24200B) Terminal Explanation



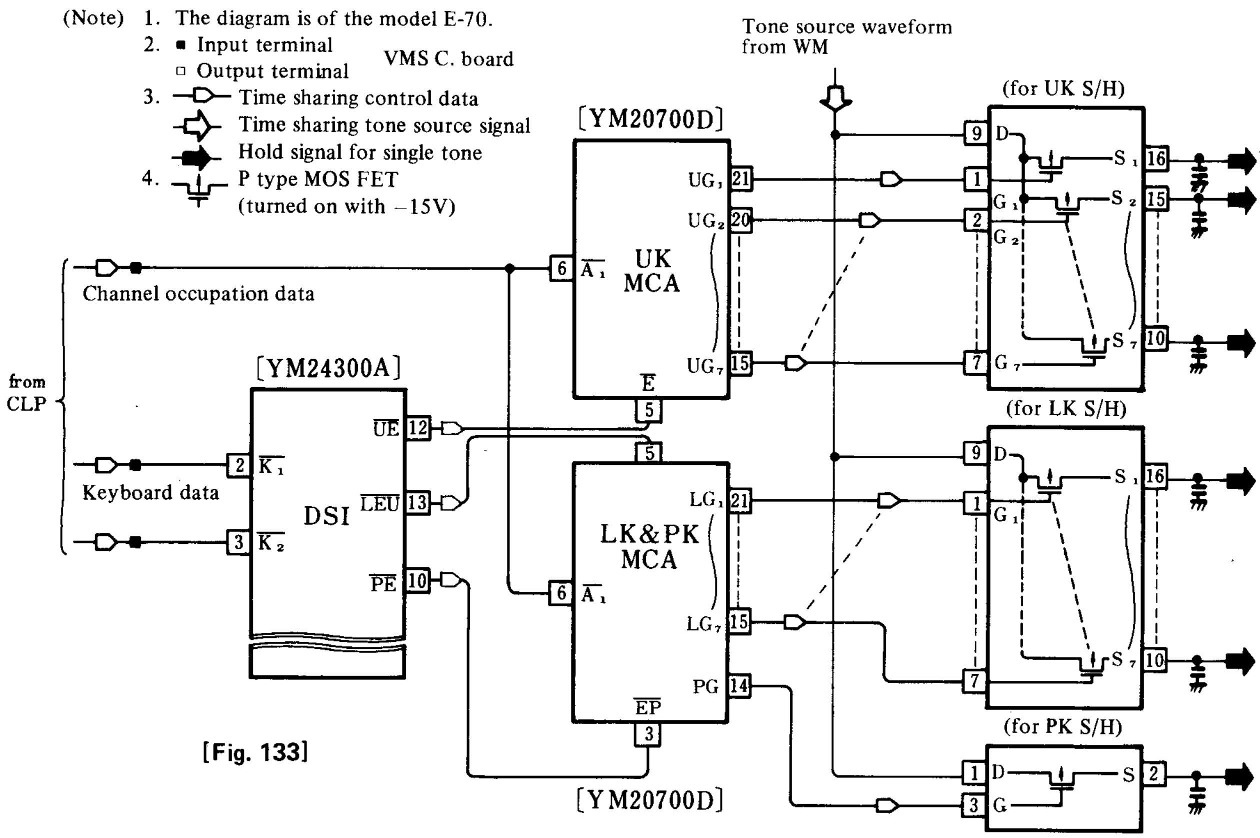
[Fig. 132]

6 — 2 ● CHANNEL DISTRIBUTION CONTROL CIRCUIT

1. Point

(1) This circuit produces the control data (gate control data for S/H circuit) to distribute the tone source signals, which are contained in respective channels, to each keyboard.

(2) The movement of S/H circuit is controlled by the output control data and the number of possible tones to sound are limited to seven (7) in order the key pressed for both or either of UK and LK tones.



[Fig. 133]

Basic Block Diagram for Channel Distribution Control Circuit (with S/H)

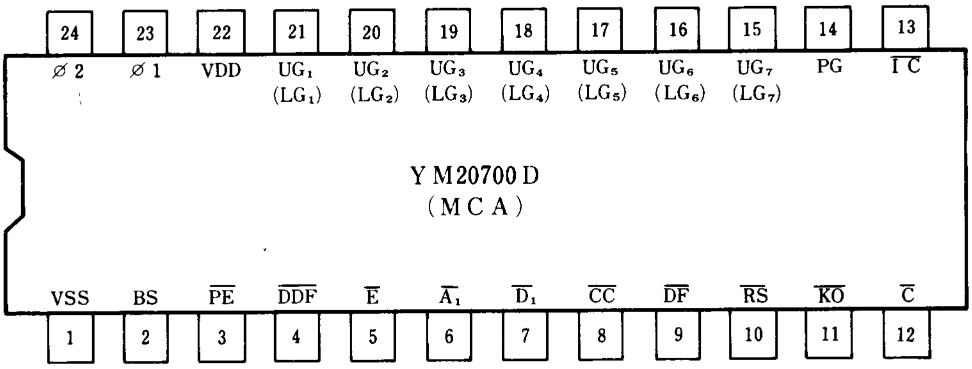
2. Basic Circuit Construction

(1) Data · Selector I [DS I: YM24300A]
Produces the enable data to move MCA (prepared to each keyboard) circuit simultaneously with each channel time.

(2) Multi Channel Asigner [MCA: YM20700D]
As a data to indicate the occupation condition of the 12 sound channels, this receives $\overline{A_1}$ data in order the first-come basis up to 7 channels for each UK and LK and 1 ch for PK and fed out gate control data.
And also has the functions of "Upper · plus · Lower" effect.

(Note) ● The MCA output data for UK and LK in this circuit are used for key voltage generation circuit to controll VCF · VCA and EG I circuit.
● The LSI of MCA has the function of repeat effect.

3. MCA (YM20700D) Terminal Explanation



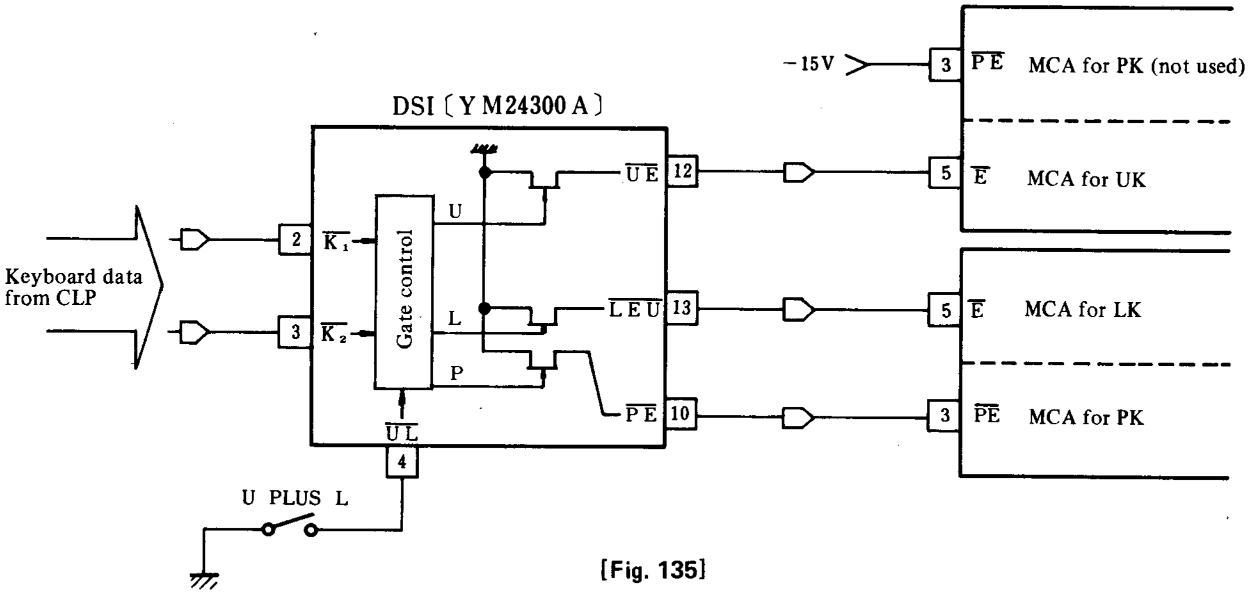
Terminal No.	Terminal Code	Designation	Significance	Terminal No.	Terminal Code	Designation	Significance
1	VSS	————	Power source (= 0V)	24	Ø 2	Master clock	f≒891kHz ϕ_1 is opposite phase from Φ_2
2	BS	Bit SELECTOR	not used	23	Ø 1	〃	
3	$\overline{PE}$	PEDAL ENABLE	for PK channel Enable data input terminal	22	VDD	————	Power source (= −15V)
4	$\overline{DDF}$	DECAY FINISH DATA	Decay finish data input terminal (from EG I)	21	UG_1 (LG_1)	GATE CONTROL DATA 1	Gate control data (chop data) output terminal for UK (LK) S/H circuit
5	$\overline{E}$	ENABLE	Enable data input terminal for UK (LK) channel	20	UG_2 (LG_2)	〃 2	
6	$\overline{A_1}$	————	Channel occupation data input terminal	19	UG_3 (LG_3)	〃 3	
7	$\overline{D_1}$	DECAY DATA	Decay data input terminal	18	UG_4 (LG_4)	〃 4	
8	$\overline{CC}$	COUNTER CLEAR		17	UG_5 (LG_5)	〃 5	
9	$\overline{DF}$	DECAY FINISH		16	UG_6 (LG_6)	〃 6	
10	$\overline{RS}$	REPEAT SPEED	Repeat speed oscillator clock input terminal	15	UG_7 (LG_7)	〃 7	
11	$\overline{KO}$	KEY-ON DATA	Key-on data input terminal (from Rhythm Driver Circuit)	14	PG	GATE CONTROL DATA PEDAL	Gate control data output terminal for PK S/H circuit
12	$\overline{C}$	CLEAR	EG I Clear data output terminal	13	$\overline{IC}$	INITIAL CLEAR	

[Fig. 134]

4. Outline of the Movement for Channel Distribution Control Circuit

- MCA is provided for each keyboard (but that of LK and PK are built in the same IC.)
  Each MCA moves only when it is in the corresponding keyboard channel time, according to the control of enable data from DSI.

(1) MCA Movement Control with DSI



[Fig. 135]

- DSI discriminates which keyboard tone is allocated to which channel time by using the keyboard data ($\overline{K_1}$, $\overline{K_2}$) sent from CLP with time sharing.
- Moreover, it feeds out the "0" level pulse (1μS) to the terminals which complies with the code of each keyboard data by actuating gates based upon the discrimination.
- These output data are enable data to move each MCA.

[Fig. 136]

DSI Movement Condition (UL = "1")	DSI Input Terminal: Input keyboard data code $\overline{K_1}$	$\overline{K_2}$	DSI Output Terminal: Enable data ("0") output terminal	MCA to move
All keys OFF	1	1	Nothing	Nothing
UK−ON	0	1	$\overline{UE}$	MCA for UK
LK−ON	1	0	$\overline{LEU}$	MCA for LK
PK−ON	0	0	$\overline{PE}$	MCA for PK

(Note)

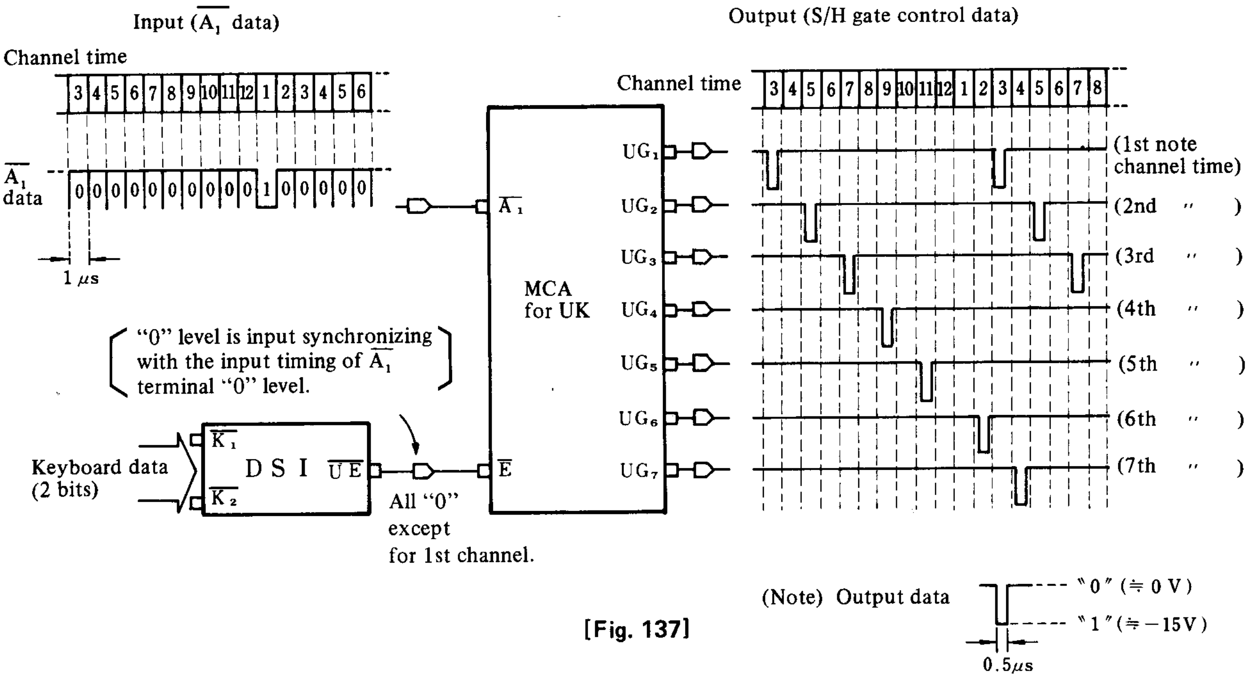
1. ... "0" 0 V; ... "1" −15 V
2. The terminal $\overline{UL}$ of DSI is usually set to "1" within the IC.

- Like this, each MCA moves simultaneously with enable data fed out from the terminals ($\overline{UE}$, $\overline{LEU}$, $\overline{PE}$) in accordance with the keyboard data of each channel.

(2) Outline of the MCA movement

- MCA receives $\overline{A_1}$ data from CLP through time sharing.
- Each keyboard MCA moves, with the DSI control, only when it is in corresponding keyboard channel time.
- Moreover, the IC of UK-MCA is so constructed to take into $\overline{A_1}$ data of channel time maximum 7 notes among the $\overline{A_1}$ data allocated to UK channel time in order the keys depressed as long as keys are continuously depressed.
- Therefore the UK-MCA receives only the $\overline{A_1}$ data which is generated synchroning with each channel time to which maximum 7 notes are allocated in order the keys depressed.
- These $\overline{A_1}$ data taken into are distributed to one of the seven output terminals without impairing each channel time and fed out as S/H gate control data for a channel time of UK. (MCA for LK is quite the same.)
- $\overline{A_1}$ data are chopped (arranged in a certain wave form) and fed out with inversion.

(Example) MCA Input-output chart when exclusively UK 11 keys are depressed.

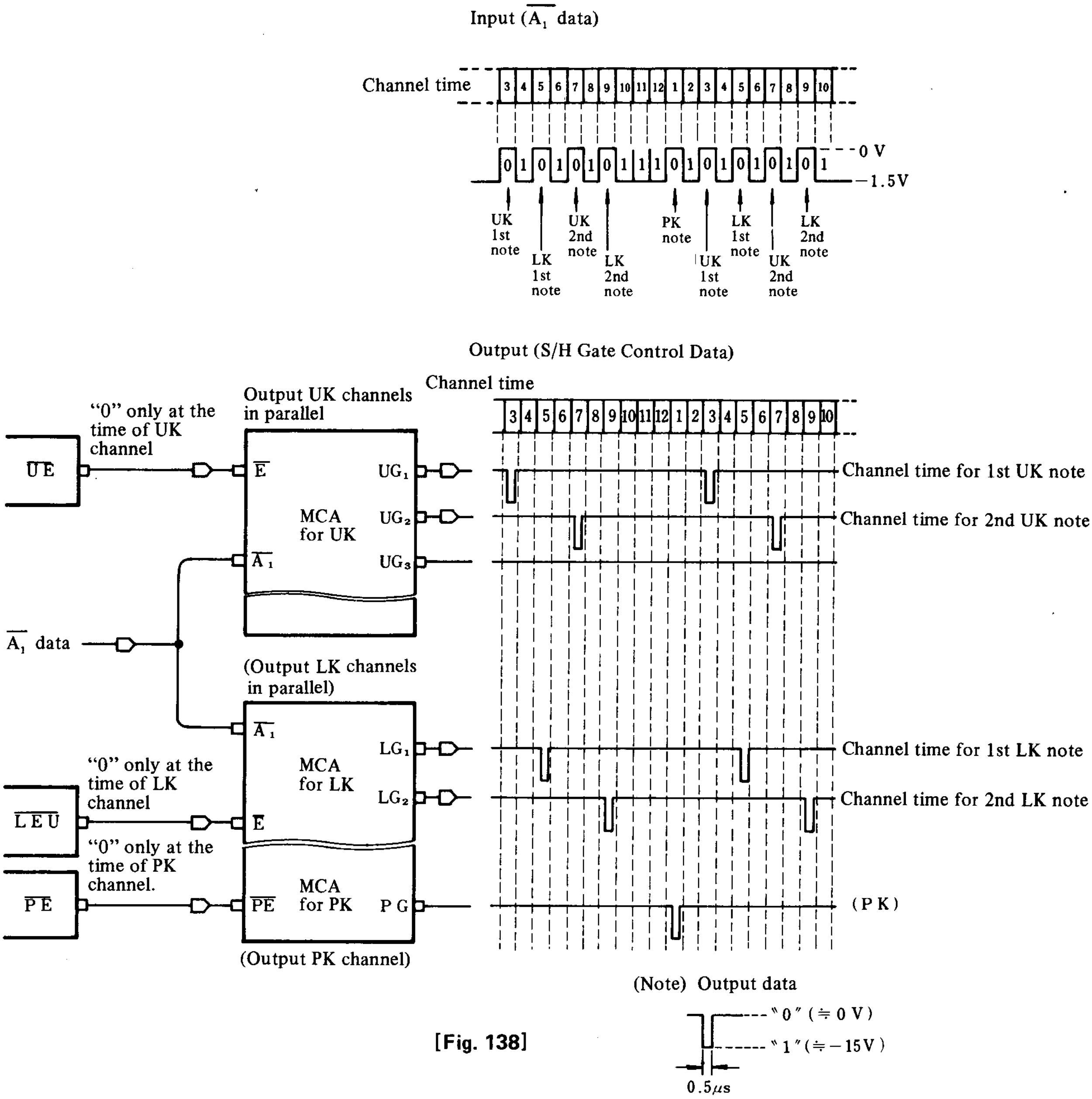


[Fig. 137]

According to the order the keys are pressed, output data of each channel time and fed out from smaller numbered terminals in order.

(Reference) Assuming that the 3rd note key is released, the $\overline{A_1}$ data corresponding to the note (allocated to 7th channel) are cleared and at the same time, the data corresponding to 8th note (allocated to 6th channel) are newly took into and fed out from UG_3 terminal of MCA simultaneously with 6th channel time.

Example 2 MCA Input-Output chart when the keys are pressed in order UK · LK · UK · LK · PK (Note $\overline{UL}$ = "1")



[Fig. 138]

The Output are appeared from the smaller numbered terminals in order without any free (empty) terminal such as, by keyboard, UG_1 (LG_1) → UG_2 (LG_2) → . . . . . . UG_7 (LG_7) from the channel time according to the order the keys are pressed.

- Since PK note is exclusivelly allocated to the 1st channel, PK MCA produces the S/H gate control data for PK by moving itself simultaneously with the timing of 1st channel.

[Reference] (Upper Plus Lower)

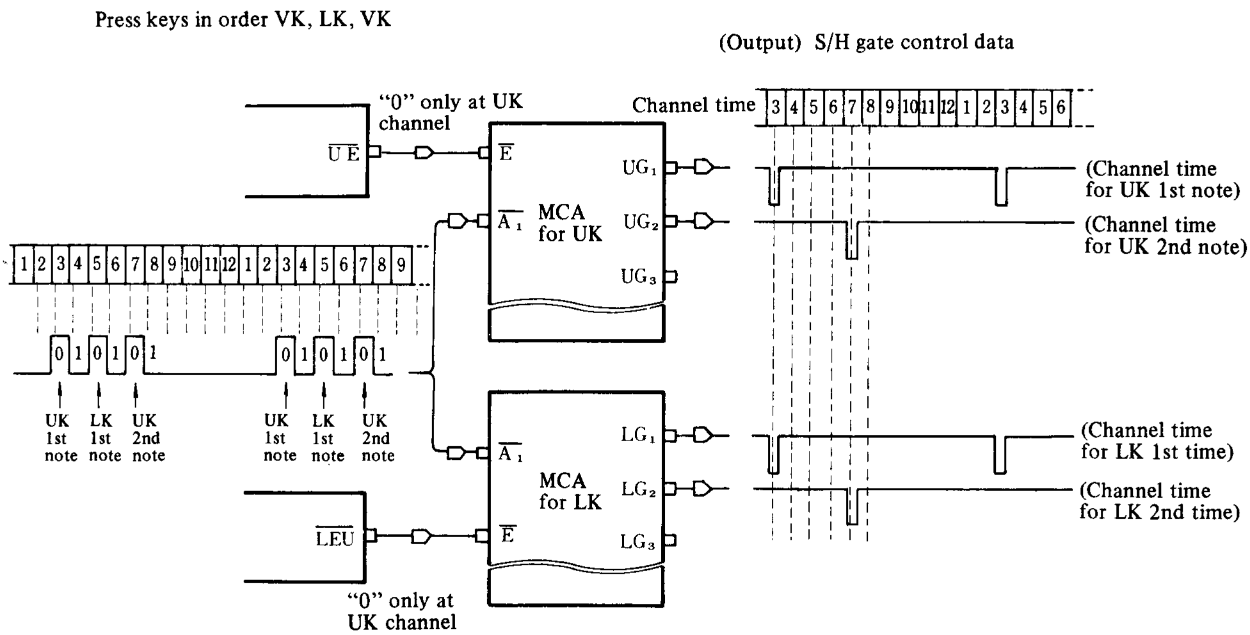
- The terminal $\overline{UL}$ of DSI can be "0" by pushing the "Upper · plus · Lower" tablet switch on E-70.
- When the terminal turns to "0", enable data to the terminal $\overline{LEU}$ can be output only under the condition that $\overline{K_1}$ = "0" and $\overline{K_2}$ = "1" (UK-ON).

[Fig. 139]

DS I Movement condition (UL = "0")	Input Keyboard Data $\overline{K_1}$	Input Keyboard Data $\overline{K_2}$	Enable Data "0" output terminal	MCA to move
All keys OFF	1	nothing	nothing	nothing
UK–ON	0	1	$\overline{UE} \cdot \overline{LEU}$	MCA for UK & LK move at a time.
LK–ON	1	1	nothing	nothing
PK–ON	0	0	$\overline{PE}$	MCA for PK

Therefore, by pressing UK key, the two MCA for UK and LK can move at a time. Consequently, the Sample Hold circuits (S/H) for both UK and LK moves simultaneously and the tone source produced by the depress UK key are added to each VCF of UK and LK so that the tone on UK as well as on LK can be sounded at the same time.

(Example 3) MCA Input-Output chart when "U plus L" switch is turned on.

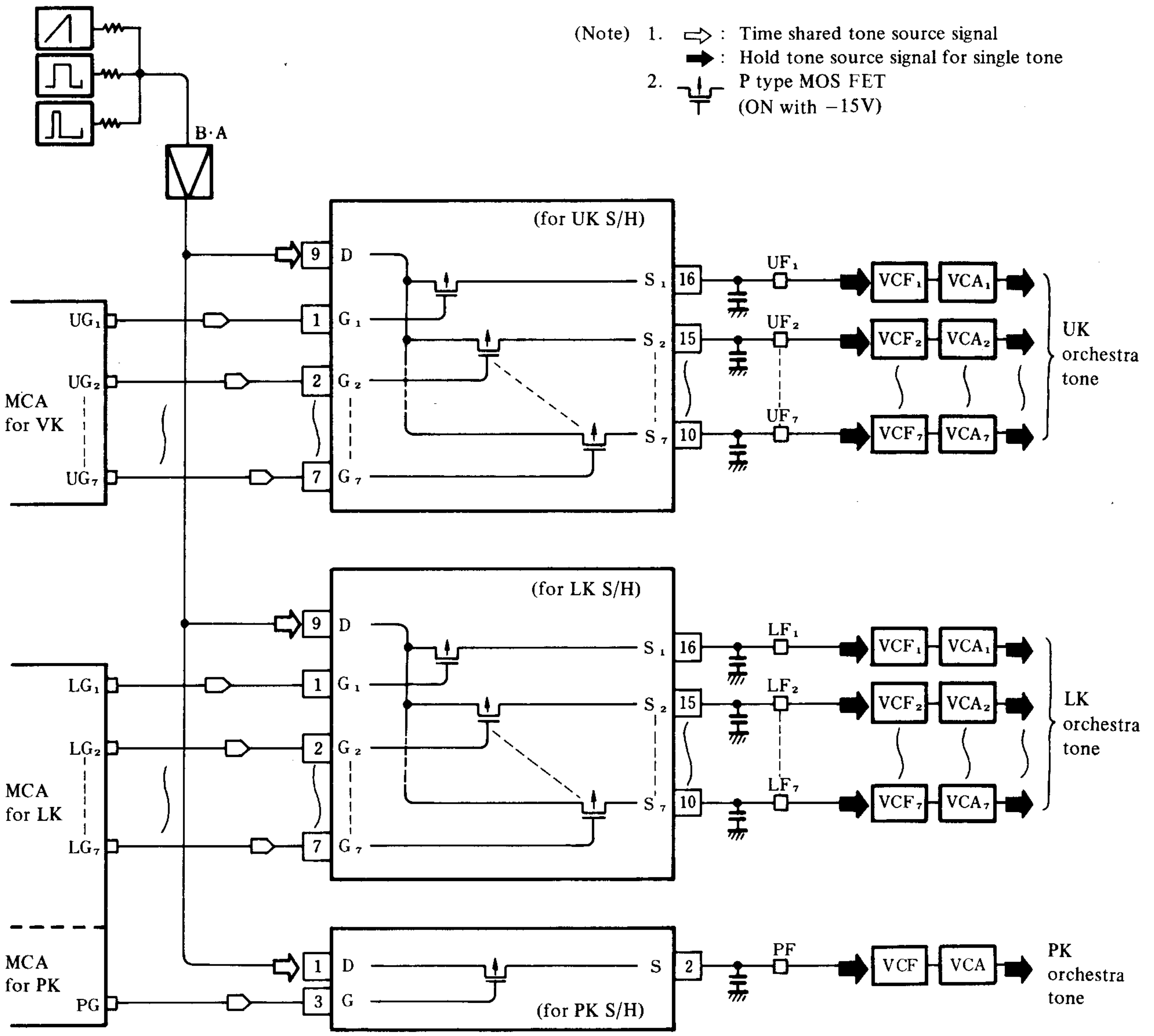


[Fig. 140]

6 — 3 ● SAMPLE HOLD (S/H) CIRCUIT

1. Point

- Carries out the gate control by making use of gate control data from MCA and sampling as well as holding the tone source signals produced through time sharing for each sanding channel.
- The gates, 7 gates for UK, 7 gates for LK and 1 gate for PK are built in to distribute to each board VCF. VCA circuit as a tone source corresponding to each keyboard.



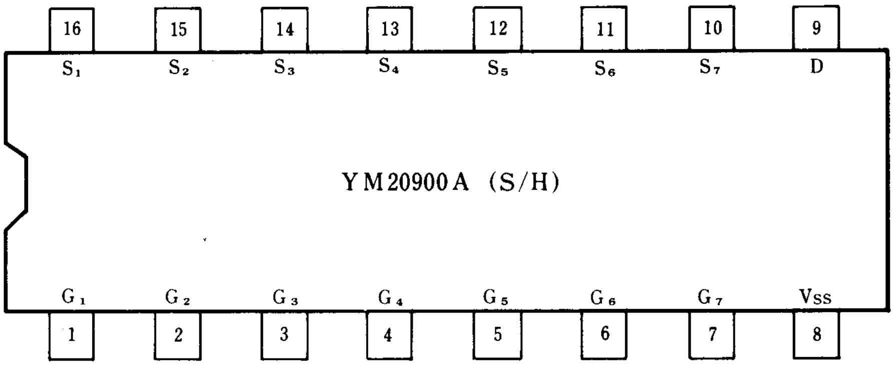
[Fig. 141]

2. The Basic Circuit is constructed with S/H Circuit prepared for each keyboard.

S/H Circuit for UK (YM20900A: with 7 gates)
S/H Circuit for LK (YM20900A: with 7 gates)
S/H Circuit for PK (TC4007P: with 1 gate)

3. YM20900A Terminal Explanation

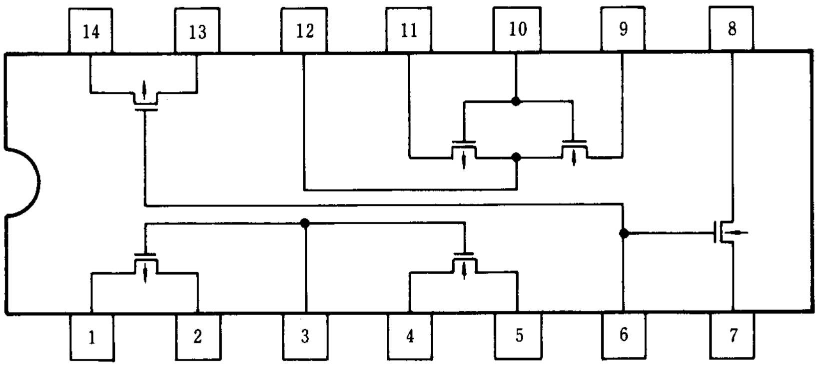
[Fig. 142]



Terminal No.	Terminal Code	Designation	Significance	Terminal No.	Terminal Code	Designation	Significance
1	G_1	GATE 1	FET (G) within IC Gate control data input terminal (from MCA)	16	S_1	SOURCE 1	FET (S) within IC signal output terminal
2	G_2	〃 2		15	S_2	〃 2	
3	G_3	〃 3		14	S_3	〃 3	
4	G_4	〃 4		13	S_4	〃 4	
5	G_5	〃 5		12	S_5	〃 5	
6	G_6	〃 6		11	S_6	〃 6	
7	G_7	〃 7		10	S_7	〃 7	
8	Vss	GND		9	D	DRAIN	FET(D) within IC signal input terminal

4. TC4007P Terminal Explanation

[Fig. 143]

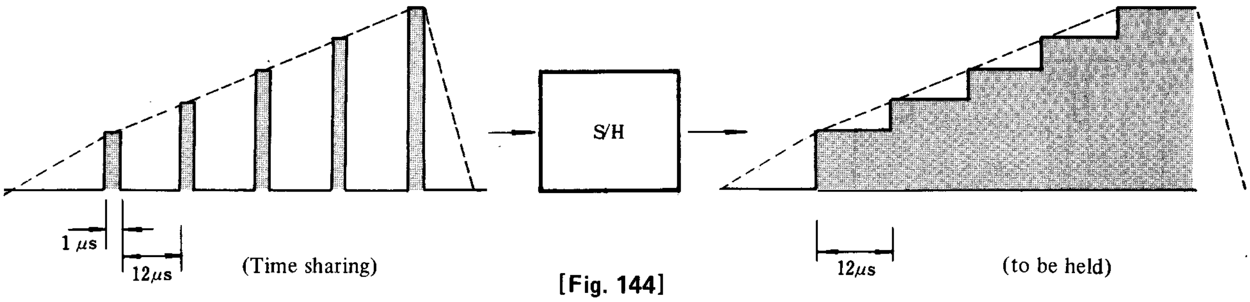


(Note) The only pins No. 1, 2, 3 are used for PK S/H circuit.

5. The Outline of S/H Circuit Movement

- Up to maximum 12 keys of tones are allocated to each channel time and fed into the terminal D of S/H circuit in a series through 12-tone time sharing.
- The IC of S/H Circuit for UK (or LK) is consisting of 7 gates circuit and respective gate movement can be controlled by gate control data from UK (or LK) MCA.
- That is, since the gate control data from MCA are the data to control each gate simultaneously with each channel time, each gate of S/H circuit can move independently synchronizing with the channel time to which a tone source signal is allocated.
- Time shared tone source signal input into D terminal of S/H circuit is, therefore, fed out from the terminals $S_1 \sim S_7$ by each channel (tone).
- The output data are held by the outside capacitor C and are sent to single tone control VCF Circuit which is provided for each tone source wave shape.

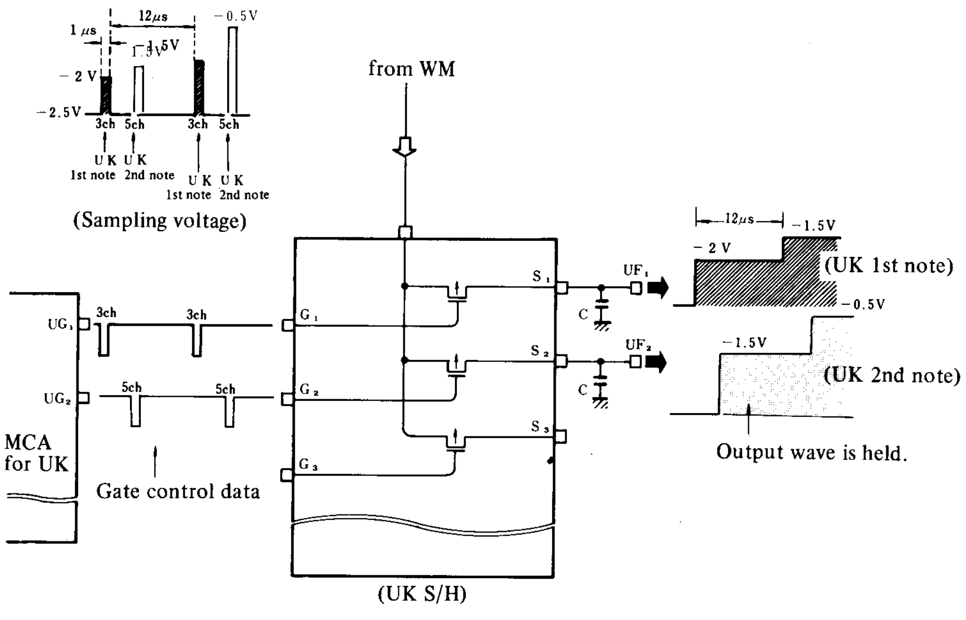
[Example] Input-Output tone source wave shape for S/H circuit



[Fig. 144]

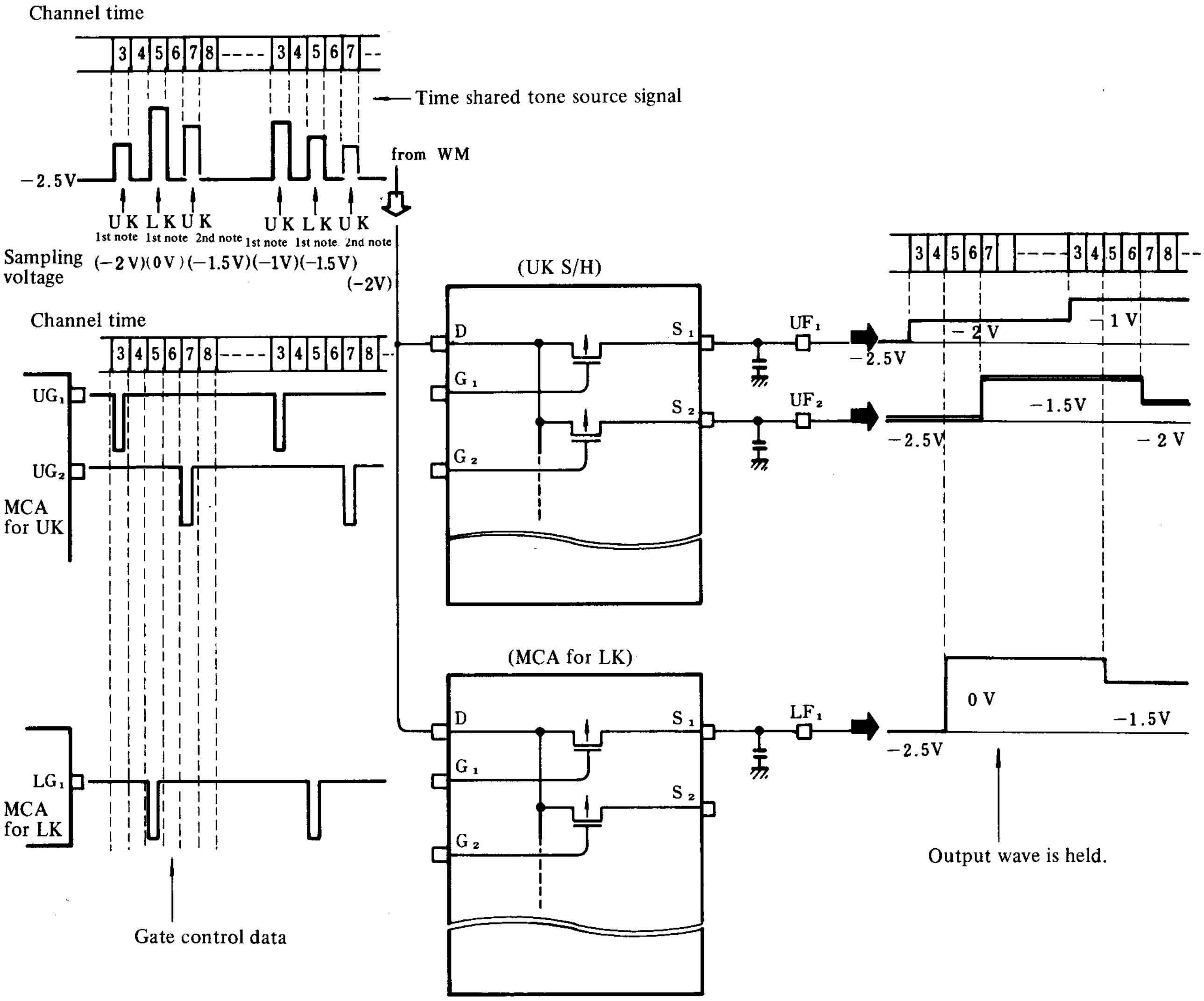
6. Example S/H Circuit Movement

(1) In the case two keys are pressed for only UK.



[Fig. 145]

(2) In the case keys are pressed in order UK, LK, UK.

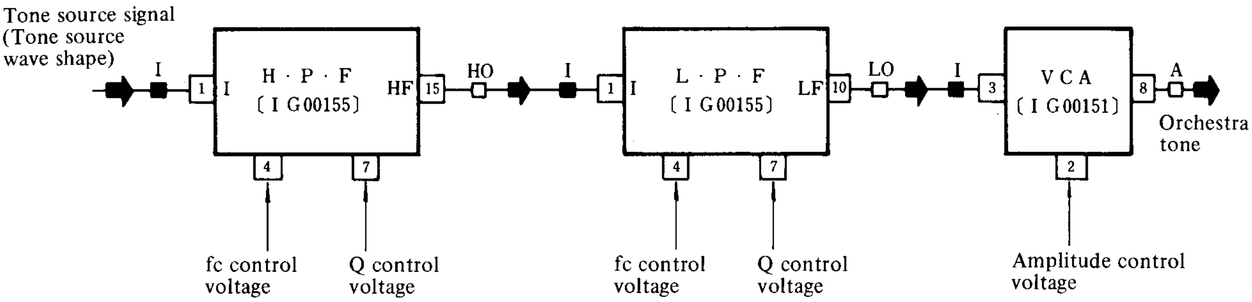


[Fig. 146]

6 — 4 ● VCF · VCA CIRCUIT

1. The Outline of VCF · VCA Circuit

- Tone color of the Orchestra tones can be created through this circuit.
  Originally, natural musical instruments have their own voices by forming the different harmonics, of it's change of attack and decay with time, and tone volume envelope. In this circuit, voltage controlled filter (VCF) by which the filter function can be controlled with voltage and voltage controlled amplifier (VCA) by which the tone volume can be controlled with voltage are used.
  By moving these circuits according to the tone selected, the more natural ochestra tones are produced.



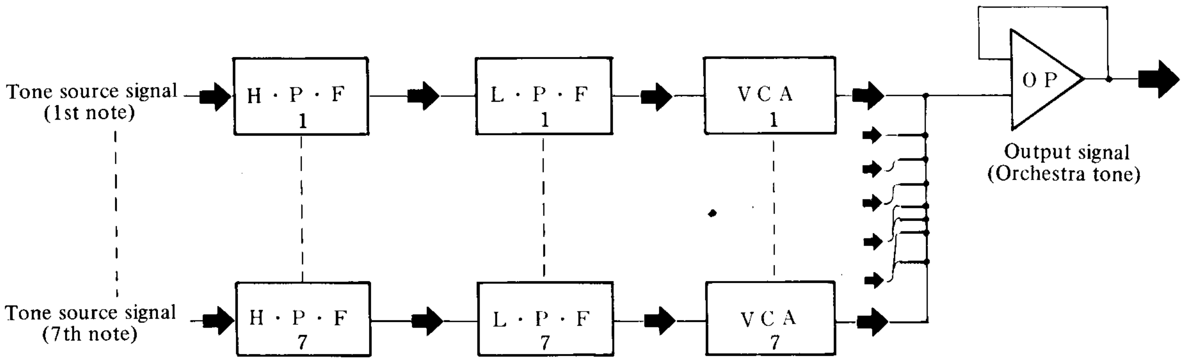
[Fig. 147]

Basic Construction of VCF · VCA

- **Basic Circuit Construction**
  (1) Voltage · Controlled · Filter (VCF: IG 00155)
  By changing the control voltage, cut off frequency (fc) and resonance (Q) can be adjusted and the overtones contained in tone source signal from S/H circuit are changeable.
  Moreover, VCF circuit take following two filter actions in order.
  - High Pass Filter (H·P·F) to pass the higher overtones than fc.
  - Low Pass Filter (L·P·F) to pass the lower overtones than fc.

  (2) Voltage · Controlled · Amplifier (VCA: IG 00151)
  By changing the control voltage, amplitude can be controlled.
  In this circuit, amplitude is controlled by the envelope voltage from VCA–EG circuit.

The basic circuits are consisting of the above circuits and they are prepared for 7 circuits (7 tones) each for UK and LK as well as 1 circuit (1 tone) for PK.



[Fig. 148]

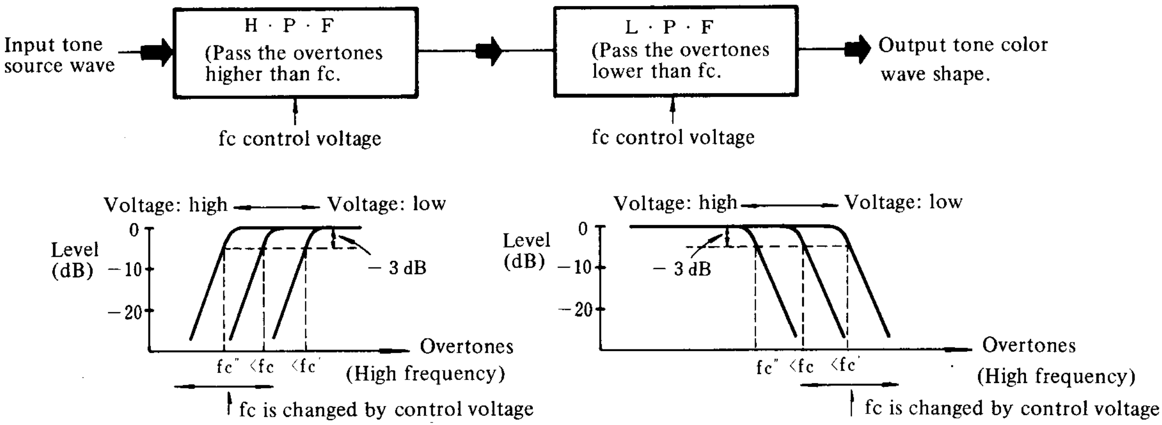
2. VCF Circuit

VCF circuit produces an aiming tone color (signal contents) with the adjustment of overtones contained in tone source signal.

(1) Principle of VCF

- Cut off frequency (fc)

  Cut off frequency of VCF circuit is controlled by the voltage added to the 4th pin of the IC (IG 00155). The lower of it's voltage, the higher the frequency becomes.



(Frequency characteristics of VCF−HPF) (Frequency characteristics of VCF−LPF)

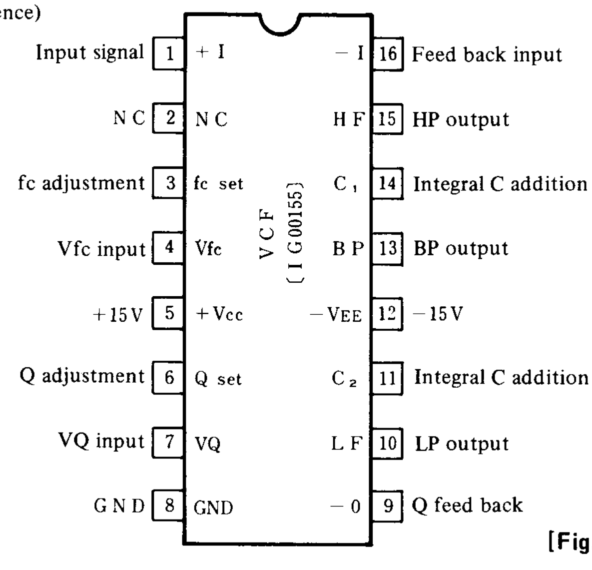
[Fig. 149]

Therefore, by changing the cut off frequency control voltage (Vfc), overtones contained in tone source signal can be varied and the tone color is changeable.

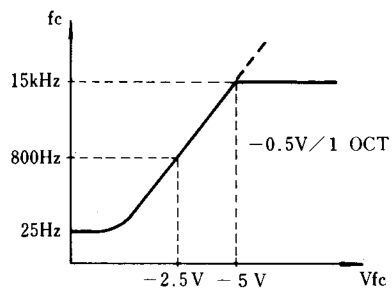
- Resonance (Q)

  Resonance accentuates the peculiar overtone in it's amplitude.
  Normally, musical instruments have their own resonance, of the same as their overtone contents.
  This VCF circuit controls the Q with the voltage added to the 7th pin (Q terminal) of IC (IG 00155).
  Therefore, in order to control the Q according to each tone color, preset voltage complying with the tone color is added to each Q terminal of HPF and LPF from respective terminals HQ and LQ of orchestra tone setting circuit (TPR 1 ~ 3 C. board) which is controlled by tone selector.

(Reference)



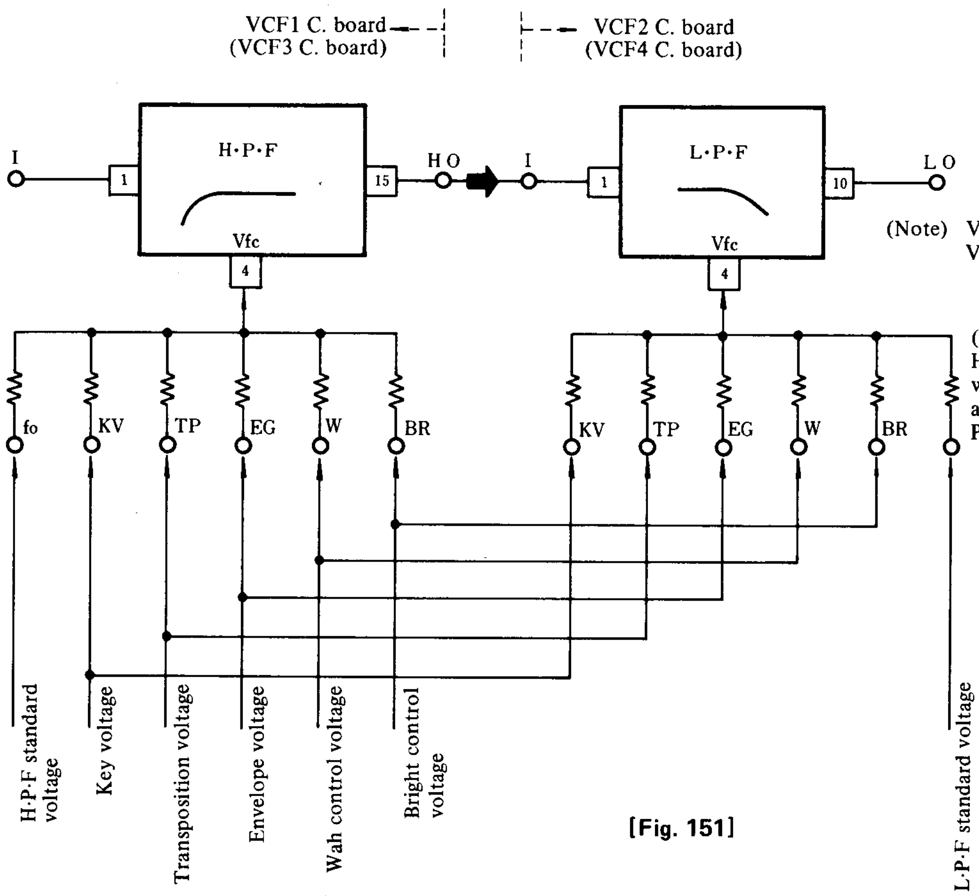
(The VCF Circuit is adjusted that fc is equal to 800 Hz when Vfc is −2.5V. This voltage is refered to an imaginary GND of VCF control voltage.)



[Fig. 150]

(2) Cut Off Frequency (fc) Control Voltage

As a voltage to control the cut off frequency of VCF circuit, the following control voltage is to each IC (IG 00155) 4th pin through Mixing.



(Note) VCF1, 2 C. board = for UK x 7
VCF3, 4 C. board = for LK x 7
for PK x 1

(Note)
H·P·F and L·P·F are provided with 7 circuits each for UK and LK as well as 1 circuit for PK.

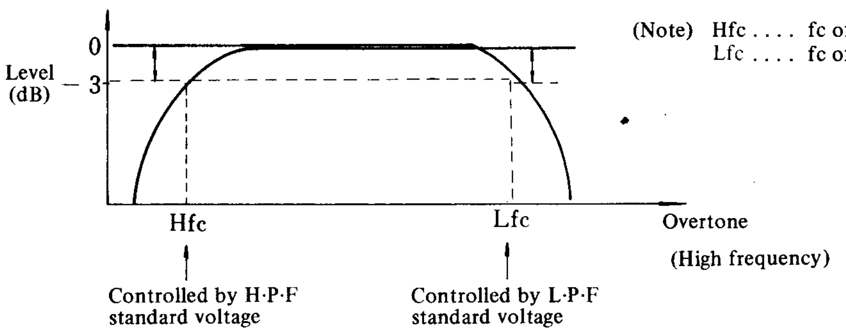
[Fig. 151]

- Standard Voltage (fo)

  To the fo terminals of H·P·F. and L·P·F., preset voltages according to each tone color selector are added respectively.

  The voltages are fed out from Hf (for H·P·F) and Lf (for L·P·F) terminals of Orchestra tone setting circuit which moves in compliance with tone color selector. Cut off frequency of VCF circuit is controlled by each voltage accordingly.

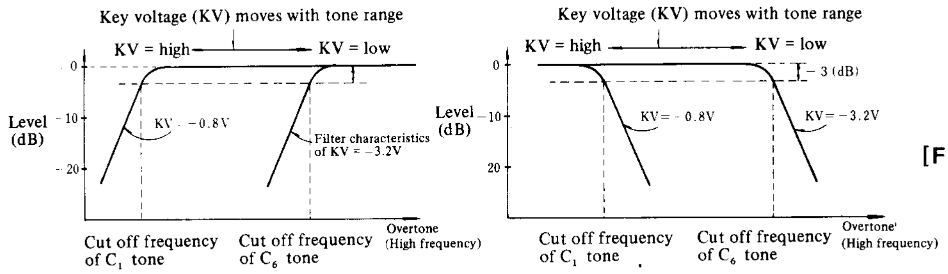
  That is, the harmonic contents (overtones) contained in the tone source signal is controlled in n accordance with the tone color selector and the preset voltage is added to compose the overtone structure for each tone color.



(Note) Hfc .... fc of H·P·F circuit
Lfc .... fc of L·P·F circuit

[Fig. 152]

- Key Voltage (KV)
  Key voltage moves cut off frequency of VCF circuit in accordance with the position (tone range) of key depressed.
  With this, an uniform overtone structure can be obtained toward any tone color and any tone range. (In other words, an identical tone color can be produced against any key.)
  This key voltage is added to the KV terminal of VCF from the key voltage generation circuit (VCG C. board) controlled by keyboard data, and fed out to the 4th pin of IC (IG 00155) after it has been mixed with fo terminal standard voltage.

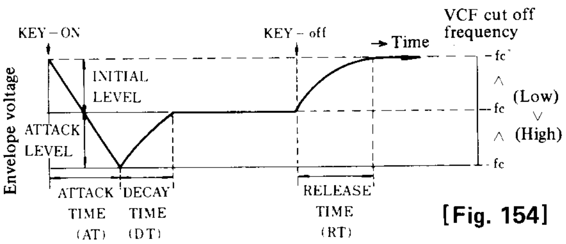


[Fig. 153]

Filter Characteristic
by VCF–HPF Voltage Control

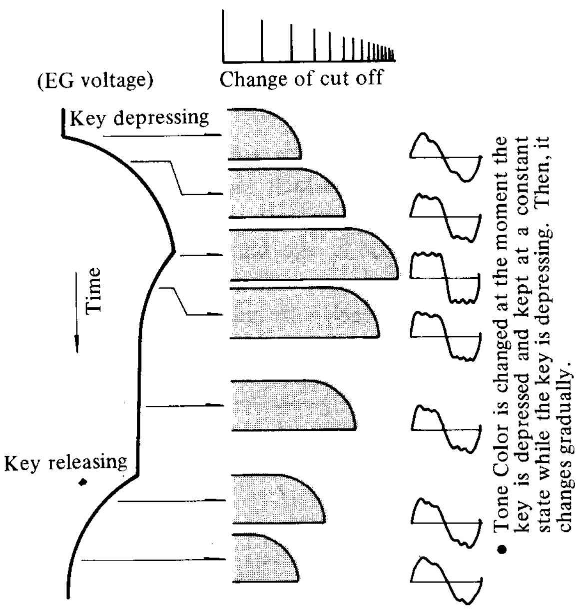
Filter Characteristic
by VCF–LPF Voltage Control

- Envelope Voltage
  Generally, the tone color of music instruments changes subtly at the moment the tone rises or decays. Envelope voltage is prepared for the control voltage to get the change of tone color with time. Envelope voltage is a time function of direct current voltage which follows the tonal locus from it's generation until disappearance.



[Fig. 154]

When the envelope voltage shown in the above figure is applied to the EG terminal as a VCF cut off frequency control voltage, the characteristics of VCF filter changes with it's cut off frequency in accordance with the moment of key depressing, during the key depressed or the state tone is decaying with key releasing.
This voltage is produced by VCF–EGI circuit (VEG C. board) which is controlled according to tone color selector, and fed out to the EG terminal of VCF circuit. (Refer to the item of EG)
Moreover, during the time the key is depressing, Sustain level is set to –2.5 volt so as not to change the tone color.

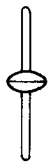


[Fig. 155]

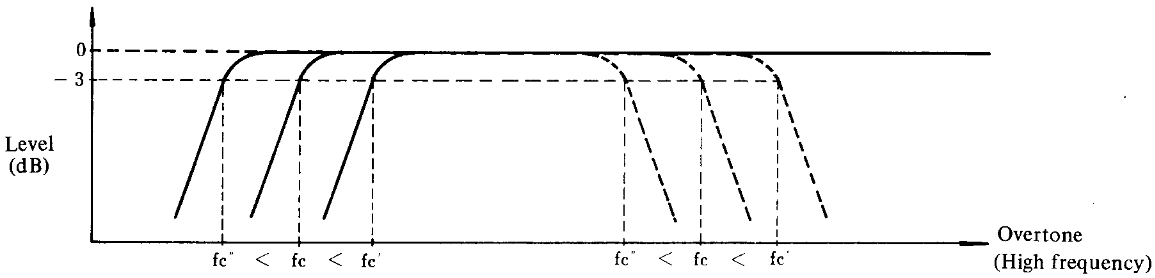
(Note) This voltage is a negative voltage within the range of 0V max ~ –5V min which deffers according to tone color.

- Transposition Voltage (TP)
  To the terminal TP of VCF circuit, the voltage corresponding to the lever position is added from the transposition circuit (TPS 1 ~ 3 C. board) which is controlled by transposition lever.
  That is, cut off frequency of VCF circuit is controlled in accordance with the feet as the same as key voltage since transposition lever is also an orchestra tone feet control lever.
  This assures a tone color to have an uniform overtone structure even in any tone range.

- Bright Voltage (BR)
  The voltage controlled by bright lever is fed into the terminal BR of VCF circuit.
  This bright lever, variable resistor with center click stop, can change the BR terminal voltage of VCF circuit within the range of −1.7V ~ 3.3V centering −2.5V. Therefore, cut off frequency of VCF circuit moves entirely based on the fc determined by standard voltage etc. with bright control lever, and the overtone contents which forms each tone color changes to be dark or to be dazzling.

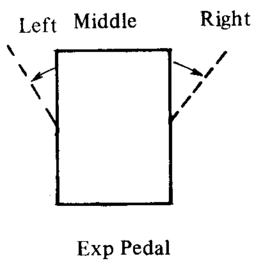
Bright lever position	BR terminal voltage	f c
	−1.7 V ↑ −2.5 V ↓ −3.3 V	fc″ ∧ fc ∧ fc′

[Fig. 156]



[Fig. 157]

- Wah Voltage (W)
  The voltage controlled by expression pedal is added to the terminal W of VCF circuit.
  This voltage can be changed by moving the pedal from side to side.



exp Pedal	Left ⟷ Middle ⟷ Right		
W terminal voltage	−1.9 V	−2.5 V	−2.9 V
Cut off frequency	fc″	< fc	< fc′
Tone color	Soft		Brilliant

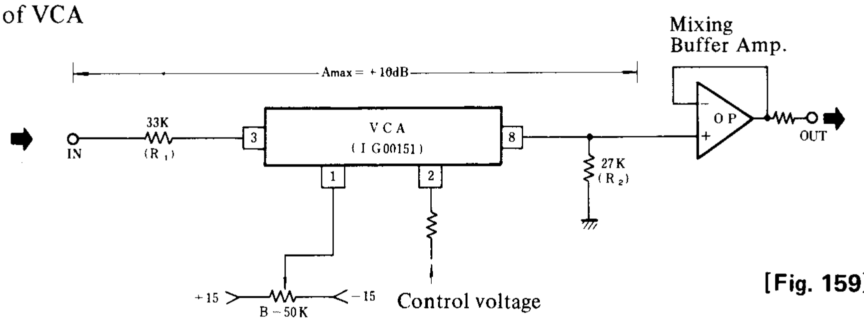
[Fig. 158]

Therefore, moving the pedal continually from side to side can change the cut off frequency of VCF circuit continually and accordingly the wah-wah effect can be obtained.

3. The Outline of VCA Circuit Movement

- In general, tones of natural musical instruments have their own tone volume envelope (change of tone volume level with time) peculiar to the musical instruments.
  This tone volume envelope is also a very inportant function to form tone of each musical instrument. By making use of the envelope voltage from VCA–EGI circuit, this VCA circuit adjusts the amplitude in order to control the tone volume envelope according to the aiming orchestra tone.

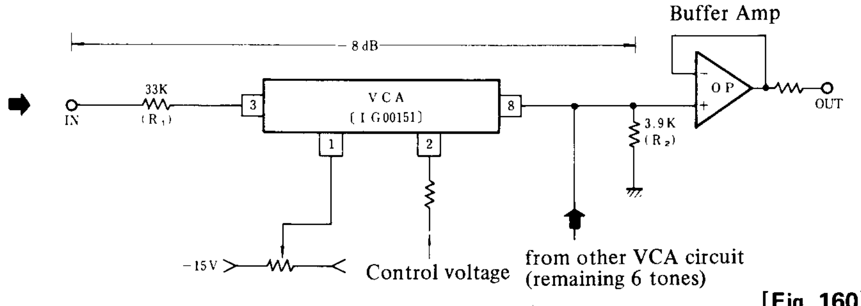
(1) Principle of VCA



[Fig. 159]

(Basic Diagram of PK VCA Circuit)

- The amplitude level of VCA (IG 00151) is controlled by the voltage added to 2nd pin of the IC and changed lineally to the control voltage.
- The above VCA circuit shows an example of the usage of PK VCA circuit in which the variable resistors (B–50K) R_1 and R_2 are adjusted, when the 2nd pin control voltage is 10V, so that the amplitude becomes 10dB (3 times). (Note: When control voltage is 0, the amplitude is also 0.)
  Therefore, in PK VCA circuit, output voltage becomes 3V p-p at the maximum control voltage (2nd pin voltage = 10V) when the input voltage is 1V p-p.
- Seven circuits (for seven tones) each are provided for UK and LK and moreover, the output from 7 circuits are mixed one another respectively.
  Therefore VCA circuit is adjusted in level with the value of R_2 being set to 3.9Ω against each a note.

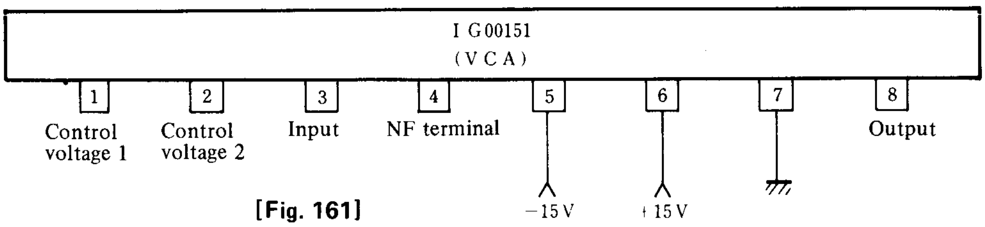


[Fig. 160]

(Basic Diagram of UK and LK VCA Circuit)

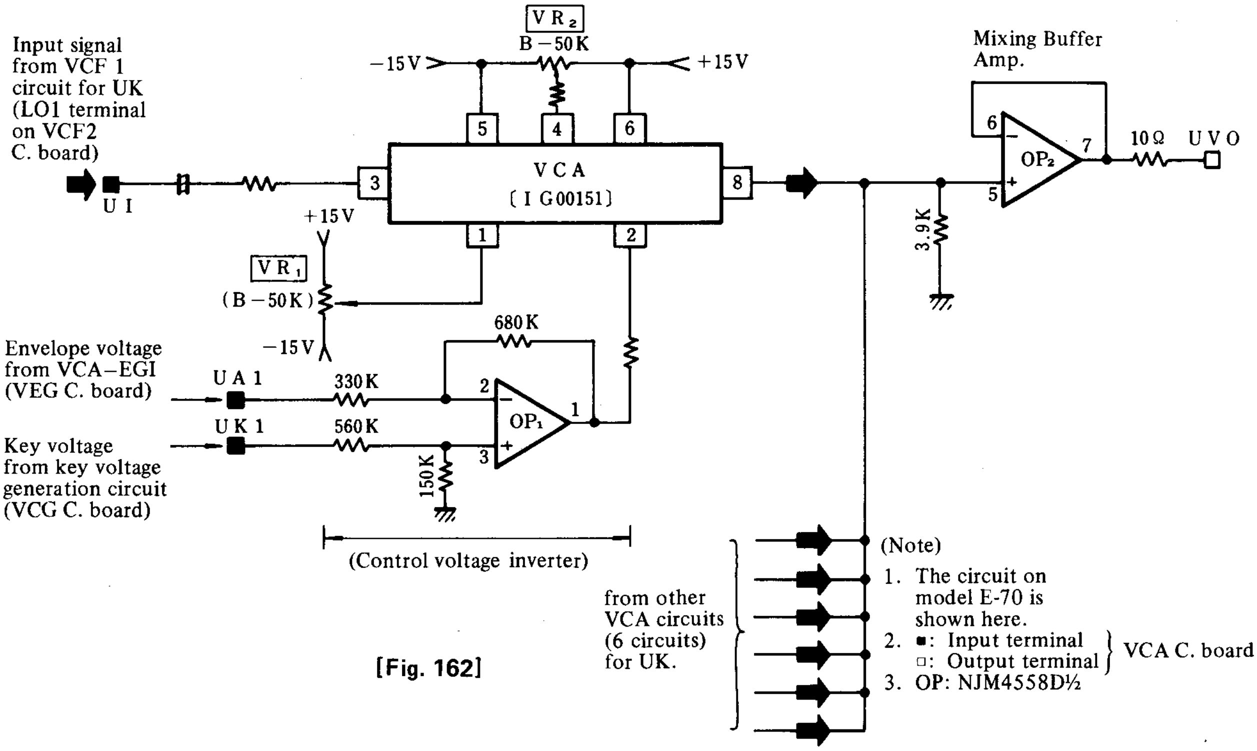
In this case one of the amplitude of VCA circuit becomes 0.4V p-p output voltage at the maximum control voltage (2nd pin = 10V) when input voltage is 1V p-p.

(Reference)



[Fig. 161]

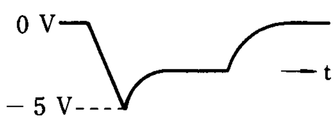
(2) Movement of UK MCA circuit



[Fig. 162]

- VCA circuit for UK is provided with seven segment circuits for seven tones and each VCA amplitude of these circuits is controlled by envelope voltage sent from VCF–EGI circuit. (VCA for LK is exactly the same as this.)
  Since the input envelope voltage is negative one from 0V max to −5V min, VCA circuit can not move with this as it is.
  Therefore, in this VCA circuit, the invertor moves with key voltage as a standard voltage is used.
  By inverting the input negative voltage (envelope voltage) the VCA amplitude control movement can be effected.

(Example of envelope voltage)



[Fig. 163]

- Envelope voltage is inverted based on the standard voltage which is divided from input key voltage by two resistors; 560K and 150K.

$$\text{OP}_1 \text{ output terminal} = \frac{150}{150+560} \times \frac{330+680}{330} \times \text{VK} - \frac{680}{330}\text{VA}$$

$$\fallingdotseq 0.65\text{VK} - 2\text{VA}$$

(Note) VA: Envelope voltage
VK: Key voltage

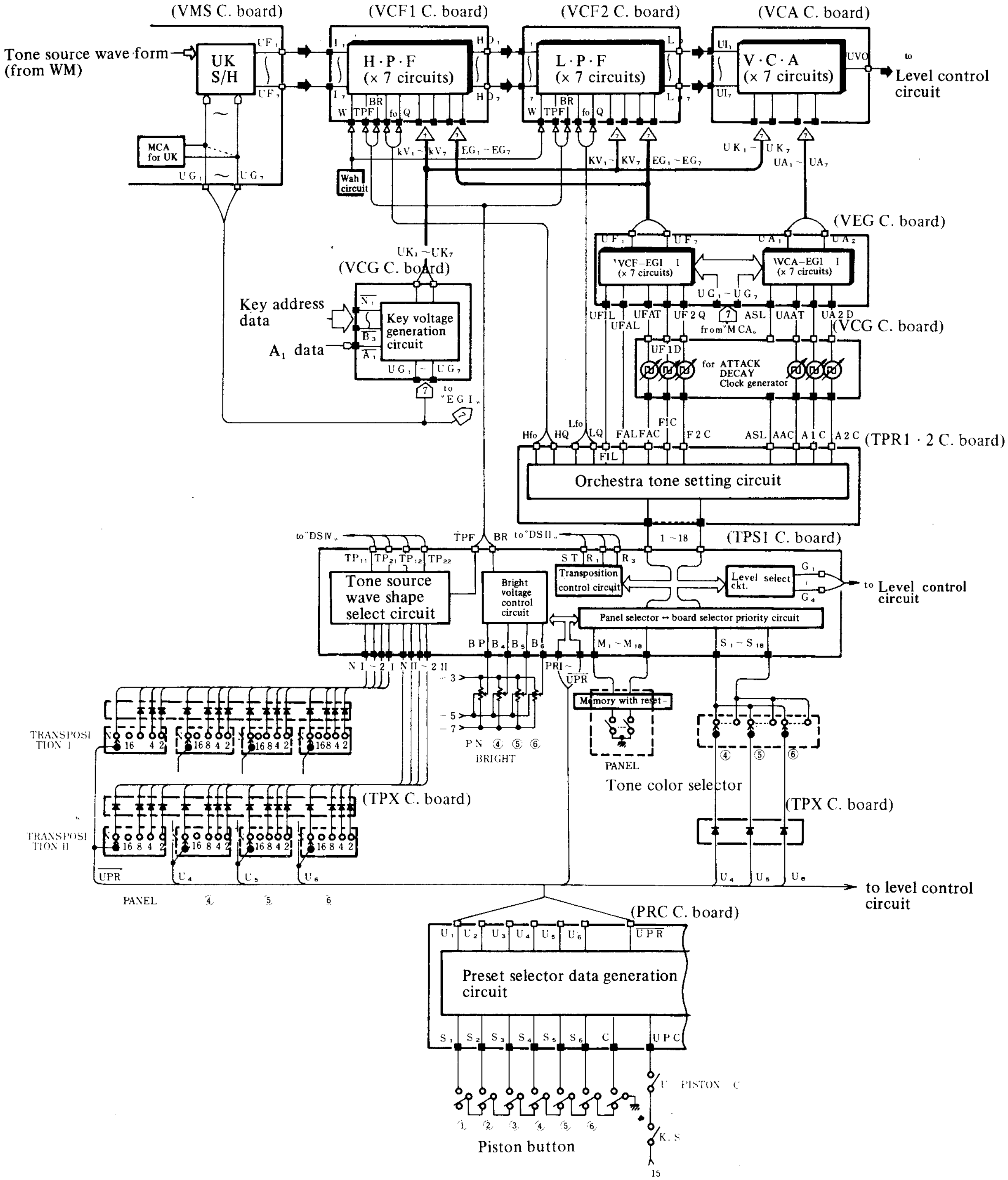
This key voltage can become high as the key with high range is depressed. (Refer to key voltage generation circuit.)
Therefore, as the key with high range is depressed, the voltage of 2nd pin in VCA is getting low and the tone volume grows down.

(Example of key voltage)

C_1	⟷	C_6
−0.8V		−3.2V

(Reference)
Since the key voltage generation circuit is not provided for PK orchestra tone, the 3rd pin of the OP amp for PK VCA invertor is grounded to GND through the resistor 150K.
Therefore, the standard voltage is fixed to 0V and the amplification control is carried out following the envelope voltage. (This is regardless of the tone range.)

6— 5 ● VCF · VCA CONTROL CIRCUIT

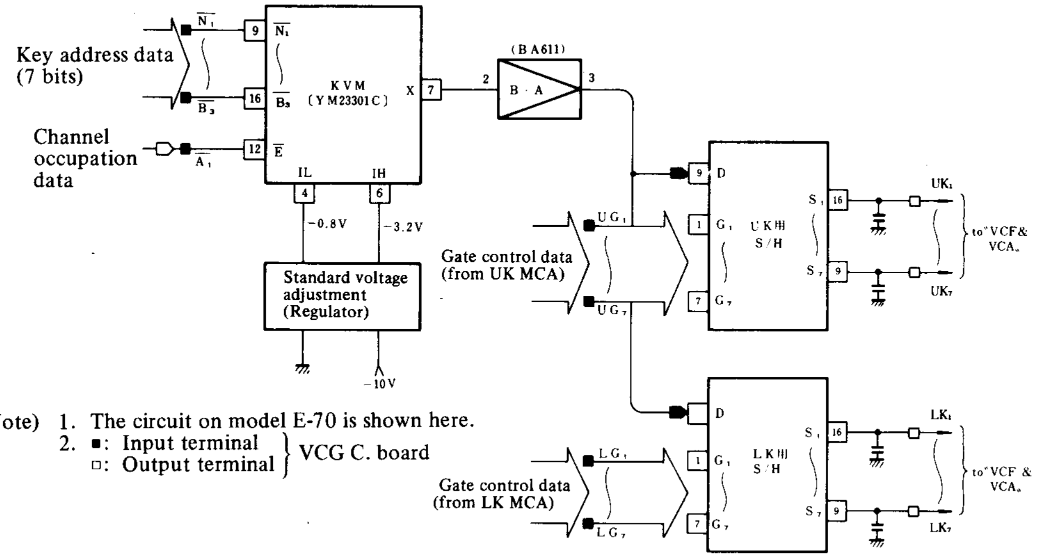


(Basic Block Diagram for VCF · VCA Control Circuit on UK) [Fig. 164]

1. Key Voltage Generation Circuit

(1) Key voltage generation circuit is composed of the following circuits.

- Key Volt Memory (KVM: YM23301C)
  Memorizes in advance the key voltages complying the 61 notes ($C_1 \sim C_6$) and output the voltage in accordance with the key address data ($\overline{N_1} \sim \overline{B_3}$: 7 bits) corresponding to the key name.
- Sample Hold (S/H: YM20900A)
  Of the key voltages fed into through time sharing, receives key voltage up to maximum 7 channels (for 7 tones) and hold them after distributing to each channel.

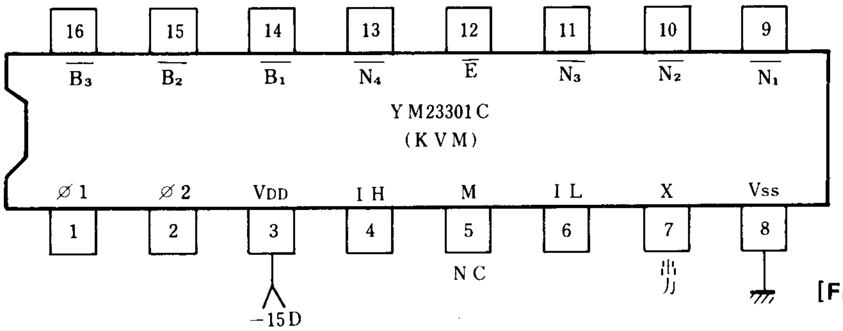


(Note) 1. The circuit on model E-70 is shown here.
2. ■: Input terminal } VCG C. board
□: Output terminal

[Fig. 165]

(Block Diagram of Key Voltage Generation Circuit)

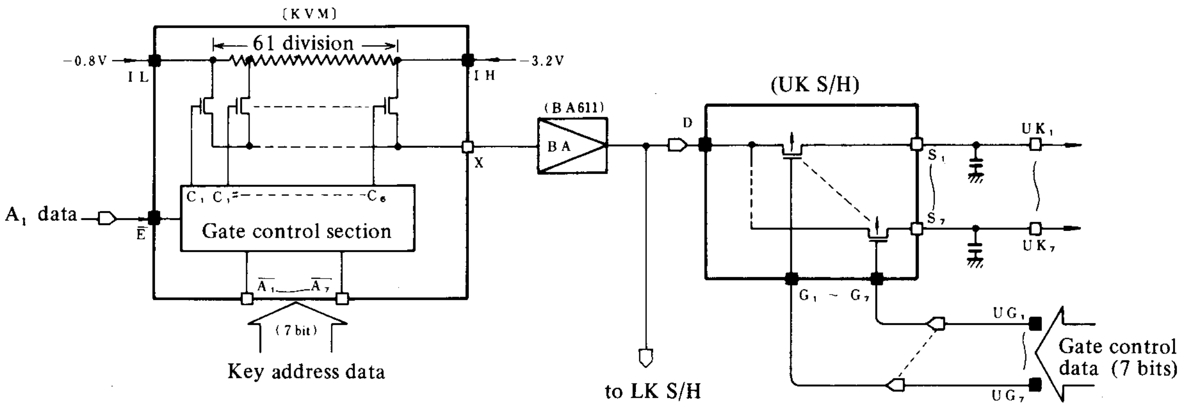
- **Reference**



[Fig. 166]

No.	Terminal		No.	Terminal	
1	Ø1	Master clock (f ≒ 891 kHz)	9	$\overline{N_1}$	Key voltage reading data (Key address data) Input terminal
2	Ø2	ϕ_1 is opposite phase from ϕ_2	⟨	⟨	
4	IH	Standard voltage high input terminal			
6	IL	Standard voltage low input terminal			
12	$\overline{E}$	IC movement control terminal	16	$\overline{B_3}$	

(2) The outline of key voltage generation circuit movement.
KVM divides in advance the voltage between the terminal I_H and I_L into 61 voltages equally. These divided sampling voltages can be fed out in accordance with 7-bit code data input into $\overline{N_1} \sim \overline{B_3}$ terminals.



[Fig. 167]

Key address data ($\overline{N_1} \sim \overline{B_3}$: 7 bits) which indicates the key name depressed are fed into the terminals $\overline{N_1} \sim \overline{B_3}$ of KVM in the key voltage generation circuit simultaneously with the channel time corresponding to each key.
Therefore, the sampling voltage corresponding to the key depressed is output to X terminal through time sharing synchronizing with each channel time.
That is, this means the key voltage is detected.
In this manner, the key voltage is fed out to S/H circuit.
Two S/H circuits are provided for UK and LK each so that the key voltage, which is time shared by the gate control data from be forementioned MCA of each keyboard, are distributed by each channel and held.
By depressing a key, therefore, the key voltage (DC) can be produced according to the key.

KEY Name	C_1	---------	C_6
Output voltage	−0.8V	---------	−3.2V

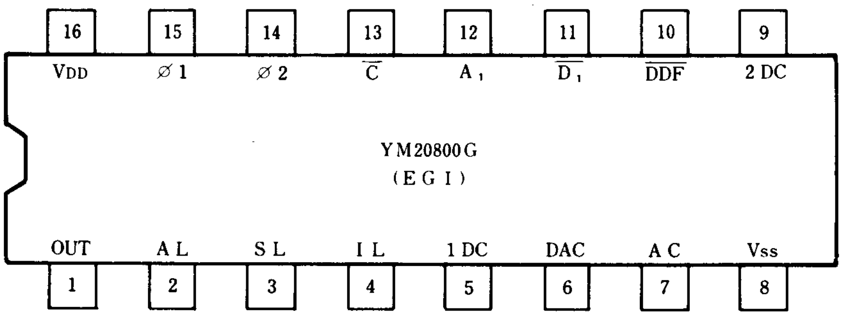
[Fig. 168]

2. Envelope Generator I (EGI)

- EGI produces the envelope voltage which changes with the passing of time from attack until decay of the orchestra tone.
  This EGI is composed of the following two circuits.
  - ○ VCF–EGI (YM20800G)
    Generates envelope voltage which control VCF cut off frequency.
  - ○ VCA–EGI (YM20800G)
    Generates envelope voltage to be added to VCA as an envelope control voltage for orchestra tone.

  And also it is provided with seven circuits each for UK and LK as well as one circuit for PK.

(1) YM20800G (EGI) Terminal Explanation

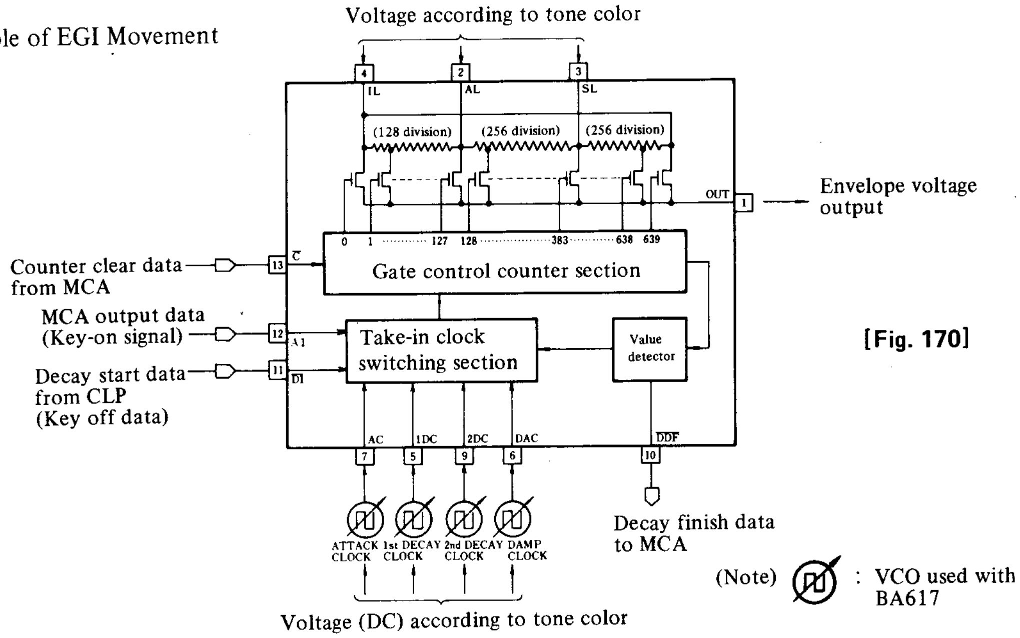


[Fig. 169]

Terminal No.	Terminal Code	Designation	Significance	Terminal No.	Terminal Code	Designation	Significance
1	OUT	OUT PUT	Envelope voltage output	16	VDD	Power source	−15 V
2	AL	ATTACK LEVEL	Attack level voltage input	15	Ø1	Master clock	f ≑ 891kHz
3	SL	SUSTAIN LEVEL	Sustain level voltage input	14	Ø2	〃	(ϕ_1 is opposite phase from ϕ_2)
4	IL	INITIAL LEVEL	Initial level voltage input	13	$\overline{C}$	CLEAR	EGI movement clear input (from MCA)
5	1 DC	1 st DECAY CLOCK	1st decay time clock pulse input	12	A_1	———	Sound data input from key on until decay finish (from MCA)
6	DAC	DAMP CLOCK	Dump clock pulse input	11	$\overline{D_1}$	DECAY DATA	Decay data input from key off until decay finish
7	AC	ATTACK CLOCK	Attack time clock pulse input	10	$\overline{DDF}$	DECAY FINISH	Decay finish data output (to MCA)
8	Vss	Power source	0 V	9	2 DC	2 nd DECAY CLOCK	2nd decay time clock pulse input

(Reference) One of the MCA output gate control data ($UG_1 \sim UG_7$ for UK) is input into the terminal. A_1 (12th pin) of each EGI during the time from key-on until decay finish.
That is, in this EGI circuit, gate control output from MCA are used as key-on data corresponding to each key and EGI (provided with 7 circuits for each keyboard) is moved one by one in accordance with each key.

(2) Principle of EGI Movement



(Block Diagram of EGI IC)

[Fig. 170]

- Within the IC of EGI, there are numerous gates to divide finely between two terminals such as 128 division for between terminals I_L and A_L, 256 division for between terminals A_L and S_L and 256 division for between terminals S_L and I_L.
  They are used to get numbers of voltages to be an oscillation width for each moment when the aiming envelope voltage wave is finely divided along with the time axis. Also, the gate control counter section counts the clock pulse of clock generator, which is accepted from take-in clock switching section, from 0 up to 639 in order, and at the same time it controls the movement of each gate in accordance with the count state.
  That is, gates between each terminals moves in order according to the number of pulse count of gate control counter and consequently the envelope voltage wave is formed by each sampling voltage.
  Moreover, take-in clock switching section accepts one of the clock pulse of four clock generators shown in the above diagram based on the following condition and feeds out it to the gate control counter.

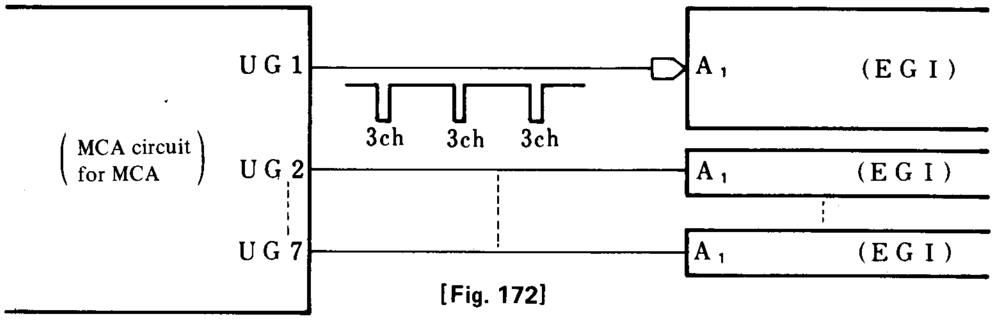
Clock acceptance condition			Take-in clock generator	Pulse count
A_1 Terminal	D_1 Terminal	(Reference)		
"1"	"1"	The moment from key-on until pulse count up to 127.	Attack Clock CK	0 ~ 127
		Automatically switches the clock when the pulse count reaches 127.	1st Decay ClockK	128 ~ 383
"1"	"0"	When key is off after 1st decay.	2nd Decay ClockK	384 ~ 639
		When key is off during 1st decay	Damp Clock K	~ 383

[Fig. 171]

(Note) A_1 terminal of each EGI is connected to a chop data output terminal of MCA circuit. The level "1" data is, therefore, input into the terminal A_1 of an EGI only when it is corresponding to the channel time of the very key during the period from the beginning until final portion of a sound. Moreover, the time shared data from CLP circuit are input into the terminal $\overline{D_1}$ during the time from key-off until decay finish. Therefore, when more than 2 keys are depressed though more than 2 tones (2 channels) of data are fed into the same EGI, each EGI detects only the $\overline{D_1}$ data of the channel which synchronizes with the channel time of the data fed into A_1 terminal.

(3) Example of movement when only one key on UK is pressed.

- As the pulse data "1" (≒ −15V) is fed out to the terminal UGI of UK MCA circuit synchronizing with the 3rd channel time to which the key is allocated only during the time from key-on until decay finish, the A_1 terminal of EGI corresponding to the UGI terminal can be on "1" level accordingly.



[Fig. 172]

- EGI takes into the clock pulse from Attack Clock Generator as soon as the "1" level data is added to the A_1 terminal.
The attack clock pulse is counted from 0 up to 127 and at the same time gates between the terminals IL and AL are activated in accordance with the number of pulse count.
The read-out time of the voltage between IL and AL is, therefore, determined by the clock pulse width (frequency) of the Attack Clock Generator. (Attack Time)

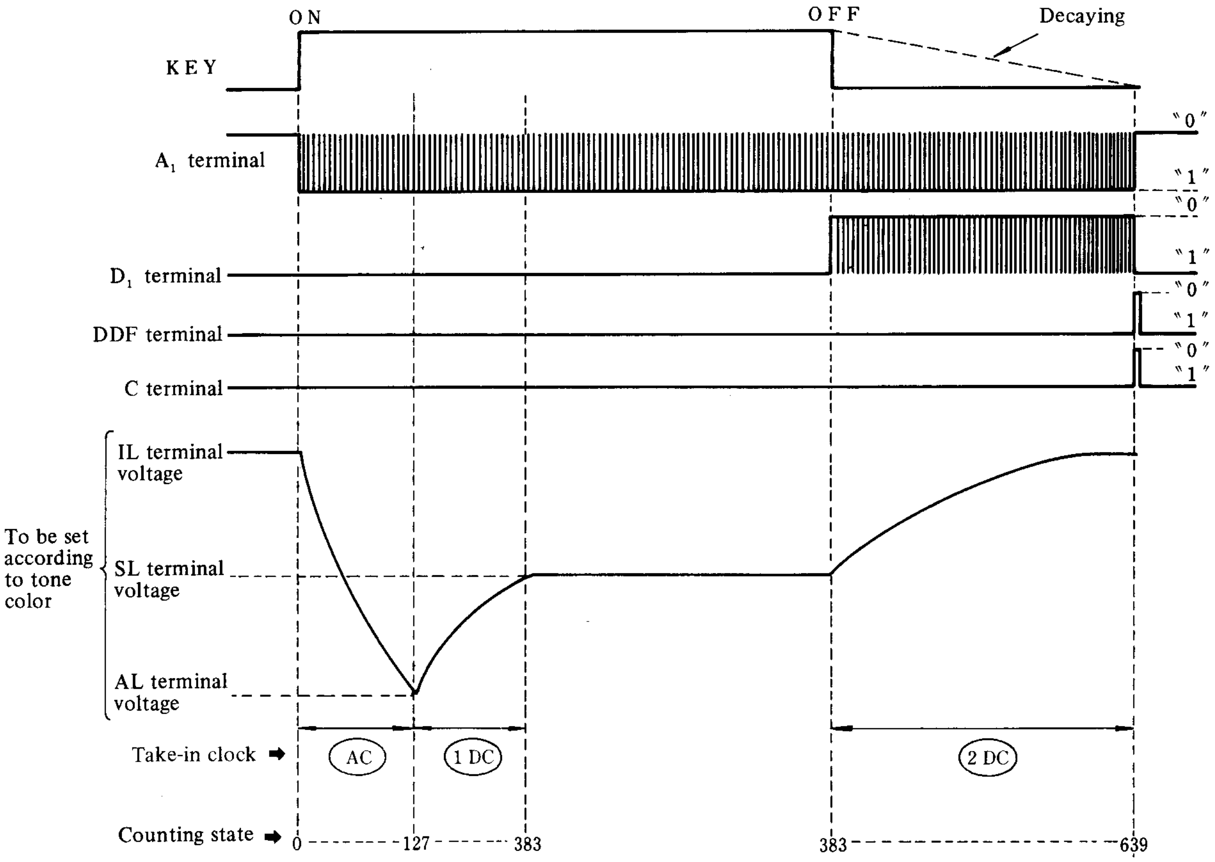
- As soon as the EGI counts the attack clock pulse up to 127 (i.e., it output the voltage at AL terminal) it switches the accepted clock to the clock pulse of 1st Decay Clock Generator automatically. Each sampling voltage between the terminal AL and SL can be read out by successively counting the clock pulse from 128 up to 383.
Therefore, the read-out time of the voltage between AL and SL is determined by the clock width (Frequency) of the 1st Decay Clock Generator. (1st Decay Time)

- When the number of pulse count reaches 383 (i.e., SL terminal voltage is output) it stops to accept the clock pulse immedicately and feeds out the SL terminal voltage continuously as long as the key is pressed. (Sustain Time)

- When the key is released, the time shared decay data ($\overline{D_1}$ = "0" level) from CLP is fed into the terminal $\overline{D_1}$ of EGI during the time from key-off until the tone dies away. EGI takes into the clock pulse from 2nd Decay Clock Generator as soon as the $\overline{D_1}$ data, which synchronizes with the channel time of input data, is fed in the terminal A_1 and reads out the sampling voltages between SL and AL by counting the clock pulse from 384 up to 639 in succession.
Therefore, the read-out time of the voltage between SL and AL is determined by the clock pulse width (frequency) of 2nd Decay Clock Generator. (2nd Decay Time)

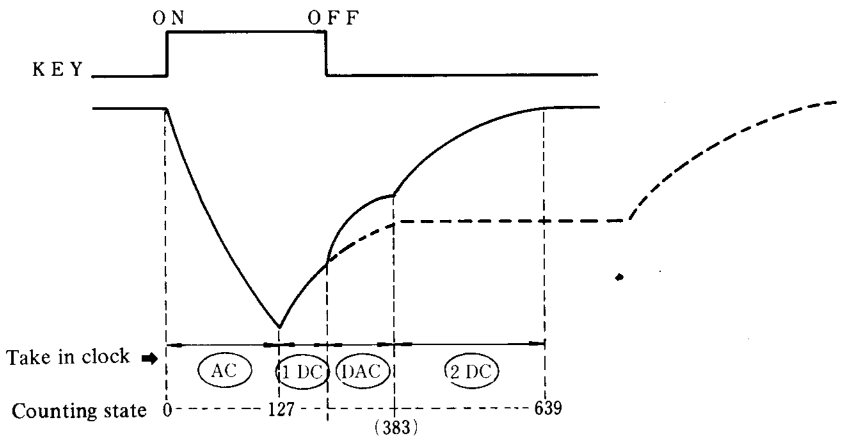
- When the count value reaches 639, the EGI output the pulse data "0" level from $\overline{DDF}$ terminal to MCA circuit simultaneously with the keys sound channel (in this case it is 3rd channel.) With the reception of this data, MCA circuit discriminates the decay finish and output the counter clear data "0" level to $\overline{C}$ terminal of EGI again to clear the EGI counter. Thus, the counter is cleared and all is returned to the first state.

(Example of Output)



[Fig. 173]

- Moreover, when the key is released during the 1st Decay Time, EGI takes into clock pulse of Damp Clock Generator in place of 1st Decay Clock at that time, and count the clock pulse successively up to 383.



[Fig. 174]

- Example of VCA–EGI

The output voltage of VCA–EGI controls tone volume envelope for orchestra tone.

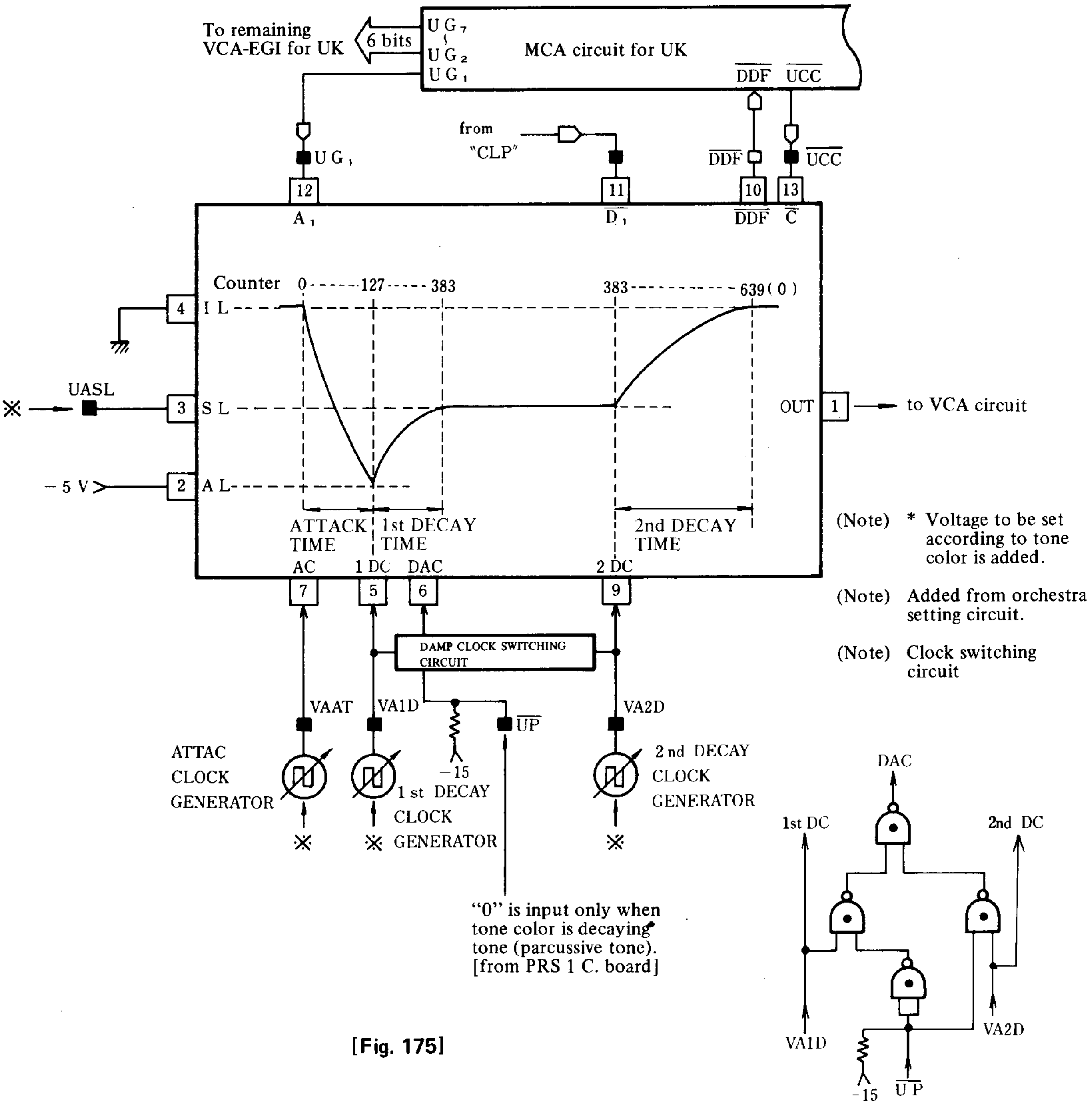
Since the voltages of the terminals IL and AL are fixed in this VCA–EGI, SL terminal voltage becomes the voltage according to the tone color selector.

That is, peak value of orchestra tone volume is fixed to a rated value so that only the tone volume level of the sustaining time is variable.

Each clock frequency is determined by tone color, but the Damp Clock, when the key is released during 1st Decay Time, can be determined by the tone color at that time.

Sustaining tone: uses 1st Decay Clock for Damp Clock

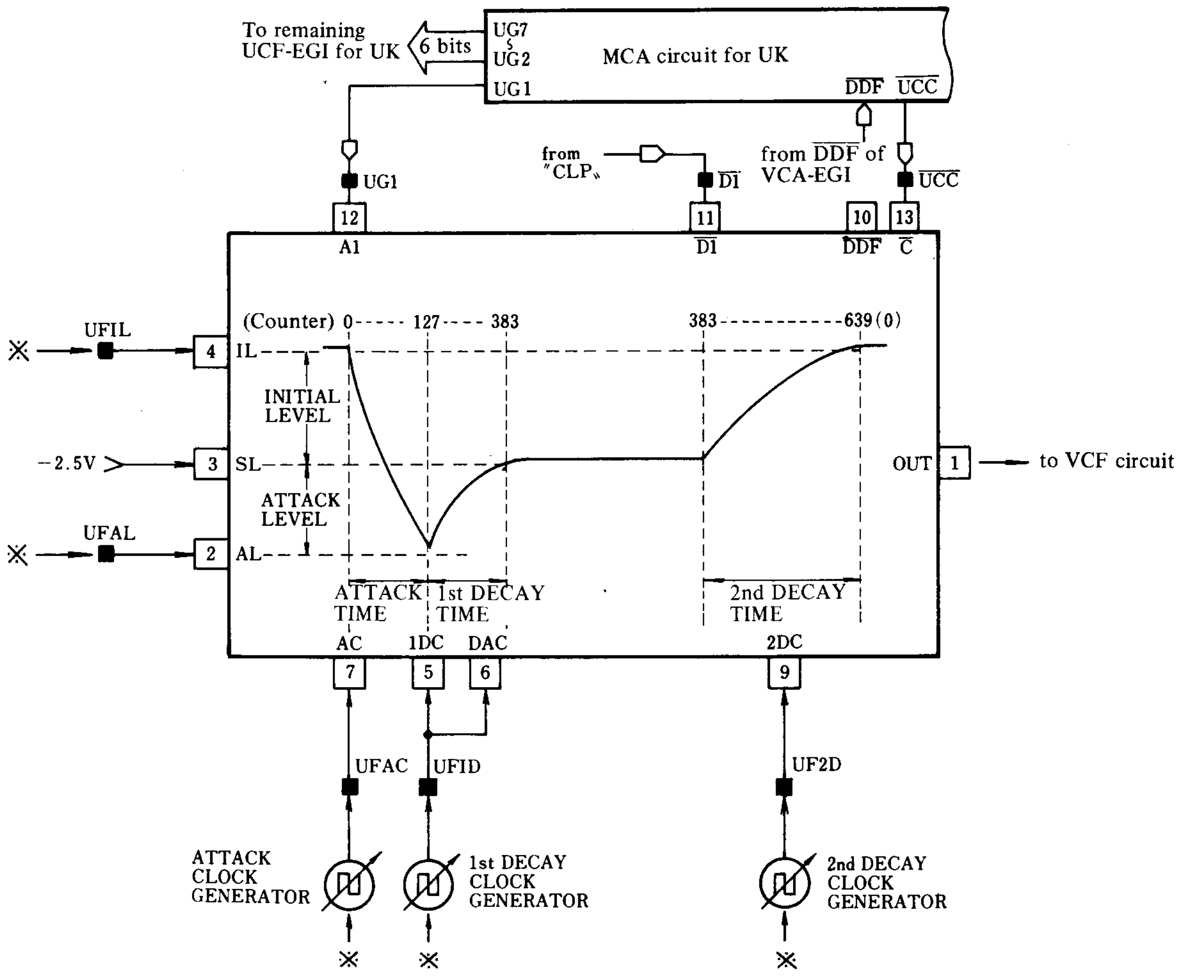
Decaying tone: uses 2nd Decay Clock for Damp Clock



[Fig. 175]

- Example of VCF–EGI output

The VCF–EGI output voltage changes the VCF filter characteristics (cut off frequency) following the key action.
Therefore, the SL terminal is fixed to –2.5V so as not to change the tone color during sustain time.
Stillmore, Damp Clock is used together with 1st Decay Clock.



[Fig. 176]

(Note) * DC voltage determined in accordance with tone color selector is sent out from orchestra setting circuit.

(Note) Output voltage wave form differs according to the tone color, because the voltage among the terminals IL, AL and SL, and the voltage to set each clock are produced by orchestra tone selector circuit respectively in accordance with the tone color. (Refer to next page.)

3. Orchestra Tone Setting Circuit

This circuit produces the voltage to control both cut off frequency and resource of VCF, each level voltage for EGI, and the voltage to determine clock generator frequency according to the tone selector.

(Note) They are built in mode E-70 as follows.
UK Tone Selector Circuit (for 18 tone colors) .... TPR 1, 2 C. board
LK Tone Selector Circuit (for 12 tone colors) .... TPR 3 C. board
PK Tone Selector Circuit (for 12 tone colors) .... TPR 4 C. board

(Note) By pressing the tone color selector, "0" (–15V) is added to the terminal only corresponding to the input terminal of the tone color.
Each control voltage is obtained by dividing this voltage.

(1) Each control voltage according to the UK tone color selector (TPR1 C. board & TPR2 C. board)

Tone color	Input \ Output	FAC	FIC	F2C	AAC	A1C	A2C	Lf	Hf	QL	QH	I	A	S	
FLUTE	1	6.00	6.40	15.0	5.44	0.67	5.70	2.01	0.26	2.36	4.59	1.51	2.63	4.66	TPR1 C. board
CLARINET	2	7.33	12.01	15.0	5.70	0.67	2.75	3.25	1.06	2.77	3.43	2.13	2.76	4.66	
TROM-BONE	3	8.97	15.0	15.0	6.41	0.67	4.13	2.84	0.28	2.38	4.45	2.07	2.62	4.66	
TRUMPET	4	8.69	15.0	15.0	6.41	0.67	4.13	3.18	0.26	2.21	4.34	2.36	2.94	4.66	
POST HORN	5	8.38	15.0	15.0	4.39	4.386	2.75	3.43	1.74	2.49	3.43	1.94	3.12	4.66	
SAXO-PHONE	6	0.67	15.0	12.6	7.33	0.67	7.71	3.86	0.26	3.33	0	2.44	3.02	4.66	

Tone color	Input \ Output	FAC	FIC	F2C	AAC	A1C	A2C	Lfo	Hfo	LQ	HQ	FIL	FAL	ASL	
OBOE	1	10.4	11.57	15	6.01	1.07	4.13	3.81	3.45	1.36	3.79	2.44	2.62	4.65	TPR2 C. board
KINURA	2	12.2	12.77	15	5.44	0.67	4.86	6.13	3.83	0	2.85	2.50	2.50	4.64	
VIOLIN	3	15	15	15	6.67	1.93	3.86	6.83	1.51	4.49	4.58	2.45	2.49	4.65	
STRING	4	15	9.46	15	6.41	2.17	5.16	6.83	2.66	2.38	4.58	2.44	2.60	4.65	
PIANO	5	0.67	15	6.41	0.67	11.3	8.04	2.10	0.63	2.56	2.23	0	3.04	0.28	
HARPSI-CHORD	6	0.67	12.6	15	0.67	11.28	8.04	6.83	2.61	2.17	4.58	2.03	2.70	0.43	
JASS GUITAR	7	0.67	12.4	15	0.67	12.60	0.67	2.12	0.65	3.84	4.58	1.19	3.93	0	
ELECTRIC GUITAR	8	0.67	11.28	15	0.67	12.60	0.67	2.89	1.73	1.17	2.97	0.89	3.97	0	
BANJO	9	0.67	15	15	1.98	8.99	8.04	4.71	0.98	1.78	2.06	0.68	4.67	0.44	
HARP	10	0.67	2.75	15	0.67	12.77	12.02	2.33	0.26	3.61	4.59	1.68	3.51	0.35	
FUNNY I	11	10.1	12.6	15	2.75	1.41	8.04	3.67	1.75	1.40	1.63	0	3.92	4.65	
FUNNY II	12	15	15	15	1.43	0.67	0.83	3.33	1.19	1.34	1.52	1.76	4.67	4.65	

Unit [– V]

[Fig. 177]

(2) Each control voltage according to LK tone color selector (TPR3 C. board)

Tone color	Output / Input	FAC	F1C	F2C	AAC	A1C	A2C	Lfo	Hfo	LQ	HQ	FIL	FAL	ASL
FULTE	1	3.86	2.05	15	6.01	2.41	2.75	2.13	0.26	2.41	4.52	2.22	2.63	4.65
DIAPASON	2	5.16	2.97	15	5.16	0.97	3.53	3.12	1.30	2.50	3.25	1.59	2.27	4.65
TROM-BONE	3	8.97	15	15	4.13	3.53	3.38	3.09	0.36	2.19	4.52	2.02	2.65	4.64
HORN	4	8.38	12.01	15	5.44	5.16	3.53	2.63	2.13	2.33	2.07	1.05	2.58	4.13
CELLO	5	8.38	15	15	5.70	2.97	3.86	5.49	0.86	4.81	4.79	2.20	2.77	4.65
STRING	6	8.38	15	15	6.41	0.67	4.99	6.83	2.01	2.63	3.76	2.02	3.05	4.65
PIANO	7	0.67	15	6.41	0.67	11.3	8.04	2.10	0.63	2.56	2.23	0	3.04	0.28
HARP	8	0.67	2.05	15	0.67	12.6	11.8	2.79	1.49	3.45	2.68	1.45	2.99	0
GUITAR	9	1.82	5.16	15	0.67	11.8	1.33	3.55	1.06	2.57	2.37	2.36	2.79	0.21
ELECTRIC GUITAR	10	0.67	5.16	15	0.67	12.6	6.67	3.05	1.17	2.76	4.55	2.46	2.83	0.06
FUNNY I	11	12.0	3.53	15	0.67	0.67	6.41	4.51	3.32	0.52	3.39	0.92	2.38	4.65
FUNNY II	12	11.81	9.48	15	0.67	4.39	5.16	4.82	2.45	0.08	0.07	1.01	3.31	4.65

Unit 〔−V〕

[Fig. 178]

(3) Each control voltage according to PK tone color selector (TPR4 C. board)

Tone color	Output / Input	FAC	F1C	F2C	AAC	A1C	A2C	Lfo	Hfo	LQ	HQ	FIL	FAL	ASL
DIAPASON	1	1.93	0.67	15	8.69	0.67	7.02	3.14	0.06	4.19	5.02	2.31	2.59	4.65
BASS CLARNET	2	3.86	12.8	15	8.97	0.67	5.44	3.68	0.04	5.03	5.01	2.42	2.52	4.65
TUBA	3	8.69	10.4	15	7.33	0.67	6.67	2.70	0.48	3.43	2.58	1.58	3.41	4.65
TROM-BONE	4	8.38	10.4	15	8.38	0.67	6.41	3.15	2.13	2.82	3.17	2.17	3.22	4.65
BOWFD BASS	5	0.67	15	15	6.67	2.55	0.67	3.98	0.19	5.03	5.02	2.21	2.63	4.65
STRING BASS	6	0.67	5.70	15	0.67	11.3	8.04	2.10	1.59	2.14	2.63	1.99	2.94	0
PIANO	7	0.67	9.46	15	1.83	11.3	9.46	2.43	1.22	4.19	4.24	0.45	3.47	0.26
HARPSI-CHORD	8	0.67	15	15	0.67	11.6	8.04	6.90	2.40	1.68	2.89	1.59	2.96	0
BASS GUTAR I	9	0.67	5.16	15	1.76	11.8	6.67	3.55	1.77	2.52	3.02	1.47	3.48	0
BASS GUTAR II	10	0.67	4.62	15	1.76	12.6	6.67	3.43	0.05	3.69	5.02	2.38	4.67	0
FUNNY I	11	0.67	7.33	15	7.33	0.67	9.68	3.63	2.22	1.48	2.05	1.31	4.67	4.65
FUNNY II	12	15	15	15	1.76	0.67	9.68	4.24	3.05	3.21	2.99	0	4.41	4.65

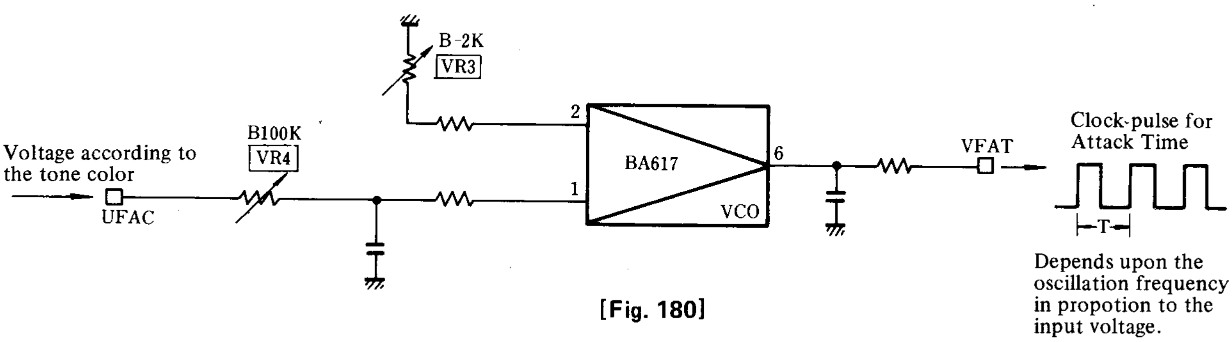
Unit 〔−V〕

[Fig. 179]

4. Clock Generator for EGI

The Clock Generator is the voltage controlled oscillator used with BA617 to determine the time required to read out EGI output voltage wave form.

(Example of the circuit for Attack Clock Generator for UK EGI)



[Fig. 180]

- The higher the voltage is input into the control voltage input terminal (UFAC), the higher the oscillation frequency becomes.

(Reference) Oscillation frequency of each clock generator is adjusted as follows with the variable resistors such as B-100KΩ on the 1 pin of BA617 is adjusted when the control terminal is in VSS (0V) while B-2KΩ on 2 pin terminal is adjusted when the control terminal is in −15V.

CLOCK GENERATOR	Output terminal	Control terminal	Control terminal voltage	
			−15V	Vss
For UK VCF ATTACK	UFAT	UFAC	115 HZ	80 KHZ
〃 1st DECAY	UF1D	UF1C	30	40
〃 2nd DECAY	UF2D	UF2C	30	40
For UK VCA ATTACK	UAAT	UAAC	115	80
〃 1st DECAY	UA1D	UA1C	30	40
〃 2nd DECAY	UA2D	UA2C	25	40
For LK VCF ATTACK	LFAT	LFAC	115	80
〃 1st DECAY	LF1D	LF1C	30	40
〃 2nd DECAY	LF2D	LF2C	30	40
For LK VCA ATTACK	LAAT	LAAC	115	80
〃 1st DECAY	LA1D	LA1C	30	40
〃 2nd DECAY	LA2D	LA2C	25	40
For PK VCF ATTACK	PFAT	PFAC	115	80
〃 1st DECAY	PF1D	PF1C	30	40
For PK VCF 2nd DECAY	PF2D	—	30	—
For PK VCA ATTACK	PAAT	PAAC	115	80
〃 1st DECAY	PA1D	PA1C	30	40
〃 2nd DECAY	PA2D	PA2C	40	40

[Fig. 181]